Communication Circuits Labs

for EE312

by

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EE312 Communication circuits lab experiments

In this set of experiments, the different electronic circuits used for communication are going to be illustrated using the simulation program Multisim already used in the previous course (EE311). You will be asked to design various circuits. The design should be performed at home before the lab session. The lab session should be spent on implementing and testing the various circuits.

When you design a circuit, you will obtain component values with a large number of significant digits. When you implement the circuit, always round the value using the closest number from the E12 or the E24 series of numbers (see the table below). For example, if you find R = 5.01 kΩ in your calculations, you should round it to 4.7 kΩ if you use 10% precision components (E12).

E24	**E12**	**E6**	**E3**
Appropriate for tolerance ±5% or narrower	Appropriate for tolerance ±10%	Appropriate for tolerance ±20%	Appropriate for tolerance wider than ±20%
10	10	10	10
11			
12	12		
13			
15	15	15	
16			
18	18		
20			
22	22	22	22
24			
27	27		
30			
33	33	33	
36			
39	39		
43			
47	47	47	47
51			
56	56		
62			
68	68	68	
75			
82	82		
91			

Table 1 Preferred List of Values for Components

2N3904

SMALL SIGNAL NPN TRANSISTOR

PRELIMINARY DATA

Type	Marking
2N3904	2N3904

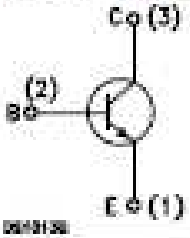
- SILICON EPITAXIAL PLANAR NPN TRANSISTOR
- TO-92 PACKAGE SUITABLE FOR THROUGH-HOLE PCB ASSEMBLY
- THE PNP COMPLEMENTARY TYPE IS 2N3906

APPLICATIONS

- WELL SUITABLE FOR TV AND HOME APPLIANCE EQUIPMENT
- SMALL LOAD SWITCH TRANSISTOR WITH HIGH GAIN AND LOW SATURATION VOLTAGE

TO-92

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	60	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	40	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	6	V
I_C	Collector Current	200	mA
P_{tot}	Total Dissipation at T_C = 25 °C	625	mW
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

$R_{thj\text{-}amb}$ *	Thermal Resistance Junction-Ambient	Max	200	°C/W
$R_{thj\text{-}case}$ *	Thermal Resistance Junction-Case	Max	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CEX}	Collector Cut-off Current (V_{EB} = -3 V)	V_{CE} = 30 V			50	nA
I_{BEX}	Base Cut-off Current (V_{EB} = -3 V)	V_{CE} = 30 V			50	nA
$V_{(BR)CEO}$*	Collector-Emitter Breakdown Voltage (I_B = 0)	I_C = 1 mA	40			V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage (I_E = 0)	I_C = 10 µA	60			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage (I_C = 0)	I_E = 10 µA	6			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 10 mA I_B = 1 mA I_C = 50 mA I_B = 5 mA			0.2 0.2	V V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 10 mA I_B = 1 mA I_C = 50 mA I_B = 5 mA	 0.65		0.85 0.95	V V
h_{FE}*	DC Current Gain	I_C = 0.1 mA V_{CE} = 1 V I_C = 1 mA V_{CE} = 1 V I_C = 10 mA V_{CE} = 1 V I_C = 50 mA V_{CE} = 1 V I_C = 100 mA V_{CE} = 1 V	60 80 100 60 30		 300	
f_T	Transition Frequency	I_C = 10 mA V_{CE} = 20 V f = 100 MHz	250	270		MHz
C_{CBO}	Collector-Base Capacitance	I_E = 0 V_{CB} = 10 V f = 1 MHz		4		pF
C_{EBO}	Emitter-Base Capacitance	I_C = 0 V_{EB} = 0.5 V f = 1 MHz		18		pF
NF	Noise Figure	V_{CE} = 5 V I_C = 0.1 mA f = 10 Hz to 15.7 KHz R_G = 1 KΩ		5		dB
t_d t_r	Delay Time Rise Time	I_C = 10 mA I_B = 1 mA V_{CC} = 30 V			35 35	ns ns
t_s t_f	Storage Time Fall Time	I_C = 10 mA I_{B1} = -I_{B2} = 1 mA V_{CC} = 30 V			200 50	ns ns

* Pulsed: Pulse duration = 300 µs, duty cycle ≤ 2 %

Lab 1

Single transistor amplifiers

Purpose

The objective of this set of experiments is to learn how to bias and test simple single transistor amplifiers. These amplifiers are used at low frequency where the intrinsic reactive elements of the transistor can be neglected.

The experiment

Part 1

In this part we are going to design a simple biasing using the 2N3904 NPN general purpose transistor. It works quite well from dc up to the VHF range. Its dc current gain h_{FE} ranges from 50 to more than 300. Its data sheet is provided above.

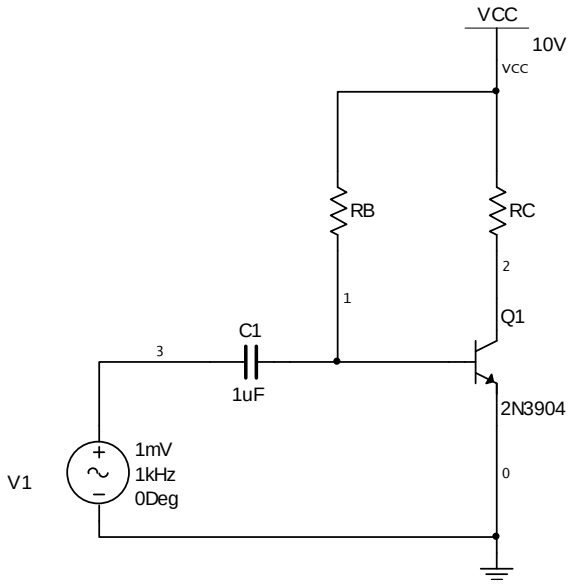


Figure 1- 1 Base Resistance Biasing

* The selected quiescent point corresponds to I_{CQ} = 1 mA and V_{CEQ} = 5 V. The power supply is V_{CC} = 10 V. Compute the appropriate values for RB and RC. Round the obtained values to a one from the E12 series. Implement the circuit on Multisim. Use an ac voltage source from the signal voltage source family. The resistors and the capacitor must be selected from the basic virtual components. The transistor on the other hand must be the 2N3904 from the NPN transistor component database. Use the multimeter to measure the dc voltage at the collector of the transistor. Compute the biasing current.

* Use the oscilloscope to measure the voltage gain. The input voltage is set to 1mV peak, 1 kHz sinusoidal. Make sure that the output voltage is sinusoidal when you perform such measurement.

* To see how the choice of the transistor influences the quiescent point, replace the 2N3904 by a BJT_NPN_VIRTUAL from the transistors_virtual family. Connect it in replacement of the 2N3904. Double click on the transistor. A window with several tabs appears. Click on the value tab, then on the edit model button. Double click on the BF value. It has the value of 100. Change it to 400 and press “enter”. Click on the change part model button and then on the ok button. Measure the collector voltage. Deduce the collector current. Repeat the same measurement using BF = 50.

* Write a small conclusion.

Part 2

In this part, we are going to use the usual resistive biasing using a single power supply and a resistive voltage divider at the base.

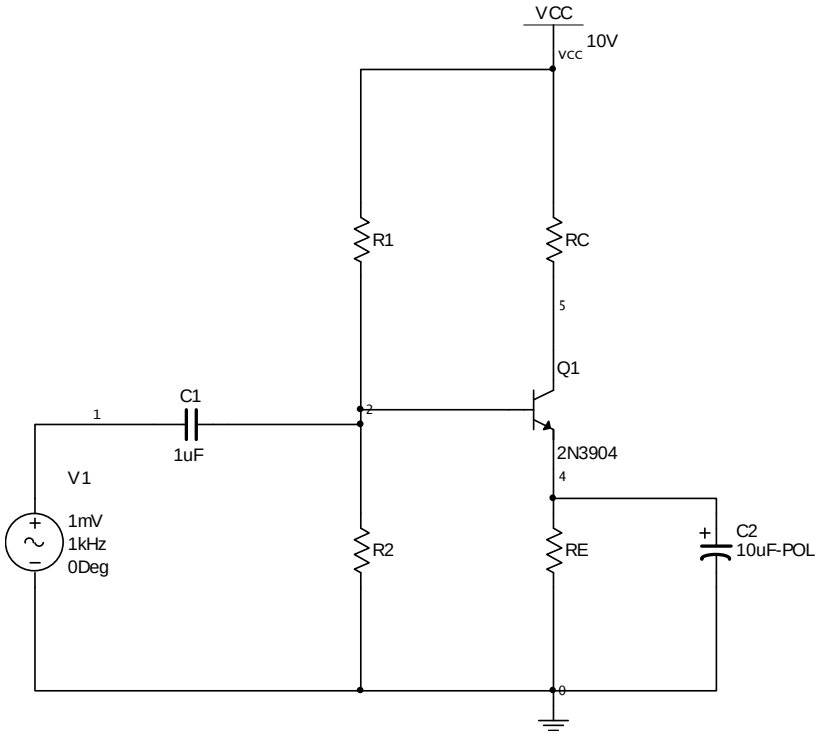


Figure 1- 2 Single supply biasing with emitter resistor

* The quiescent point is set as $I_{CQ} = 1$ mA and $V_{CEQ} = 4.5$ V (for maximum symmetrical swing). Use the rule of thumb to compute the different biasing resistances (RE, R1, R2). Compute RC in order to have the proper V_{CEQ}. The capacitors are selected so that the frequency of 1 kHz is amplified correctly. Here also, use the E12 series.

* Use the oscilloscope to measure the gain of the amplifier. Make sure that the output signal is not distorted.

* Replace the 2N3904 by a BJT_NPN_VIRTUAL as in part 1 and repeat the same measurements. What can you conclude?

* Write a small conclusion.

Part 3

In this part, we are going to use a current mirror to bias a transistor.

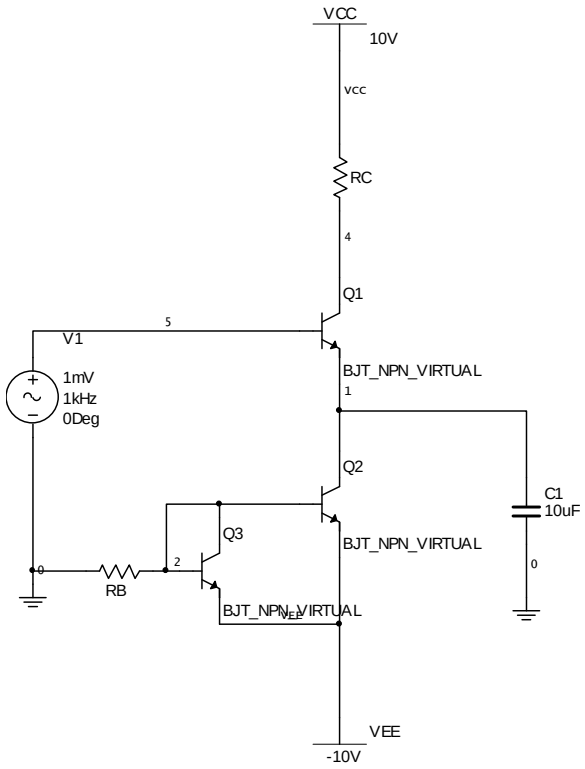


Figure 1- 3 Current mirror biasing

* Compute the value of RB in order to set the current I_{C1Q} at 1mA. Select the value of RC in order to have maximum symmetrical swing. Measure the gain of the amplifier using the oscilloscope. Increase the input voltage to 20 mV peak. Observe the output waveform. Describe its distortion.

* For this last part, we are going to use the ac analysis option of Multisim.

In the main window of Multisim, press on the Simulate menu. Select the Analyses submenu and then the AC Analysis. The following menu opens.

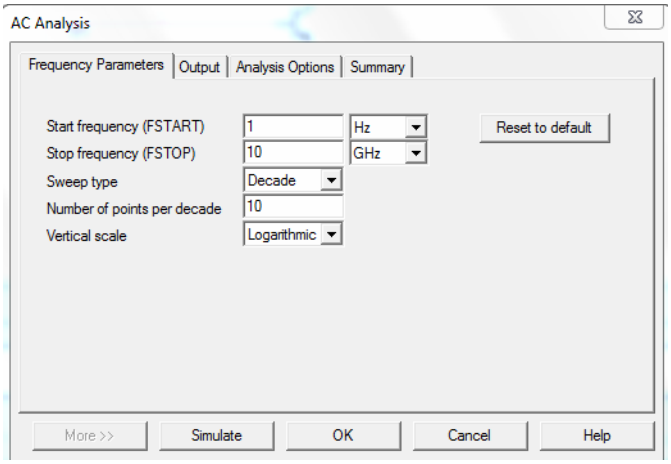


Figure 1- 4 AC analysis, Frequency parameters

Set the frequency parameters as shown in Figure 1- 4. Press the tab "Output". You will observe the window displayed in Figure 1- 5. In Figure 1- 3, the output node (collector of Q1 and resistor RC) is the node 4 (it may be different in your implementation). So, on the left of the window (Variables in circuit), press on $4, then press on the Add button (in the center of the window). On the right of the window, press on the $1. Then press on the remove button. Of course, if the output node is not 4, you must select your output node as a selected variable for analysis instead of 4.

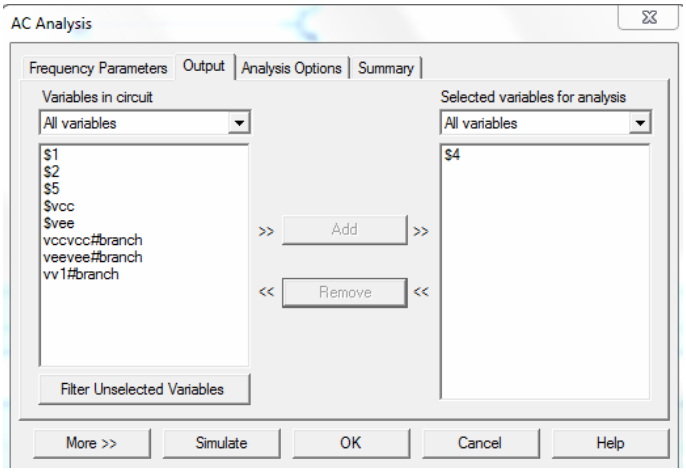


Figure 1- 5 AC Analysis, Output.

* Press on the Simulate button. A magnitude and phase response of the amplifier appears. If you want to copy one of the two curves, reverse the colors in this output window and press the copy button (to save ink). You need just the magnitude one.

* Write an overall conclusion.

Lab 2

Matching networks

Purpose

The objective of this set of laboratory experiments is to design and test simple matching networks.

The experiment

In this lab, we are going to match a resistive load of 50 Ω with a source having an internal resistance of 20 kΩ at the frequency of 1 MHz. In this particular lab experiment, use three (3) significant digits for the different components (precision better than 1%). This is due to the fact that in matching networks, people use adjustable capacitors and inductors.

Part 1

In this part, we are going to use series parallel transformations. The circuit used for matching belongs to the family of “ell” circuits. There exist four types of “ell” circuits.

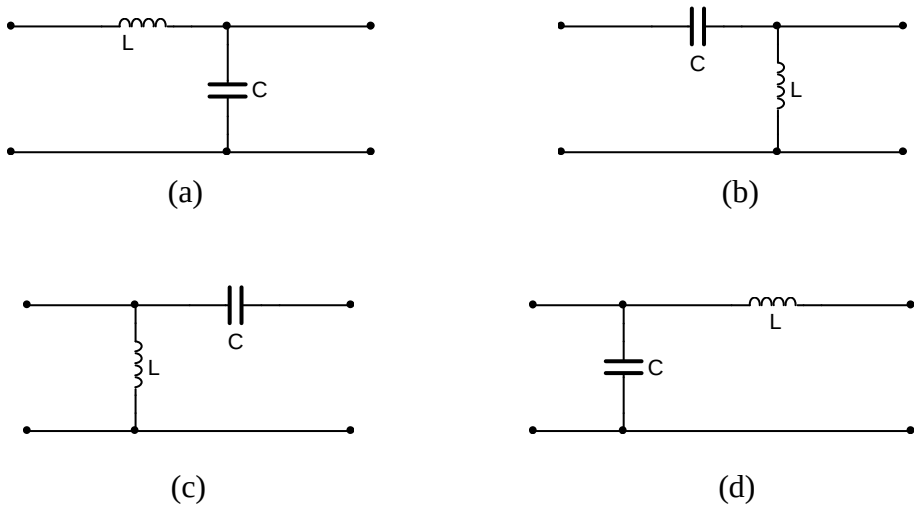


Figure 2- 1 "ell" circuits

Circuits (a) and (b) are used when the load resistance is larger than the source resistance. (c) and (d) are used when the load is smaller than the source. In our case, we are going to use the circuit (c).

Compute the required values of C and L in order to transform a 50 Ω load resistance to a value of 20 kΩ.

* Using Multisim, implement the circuit shown below (Figure 2- 2).

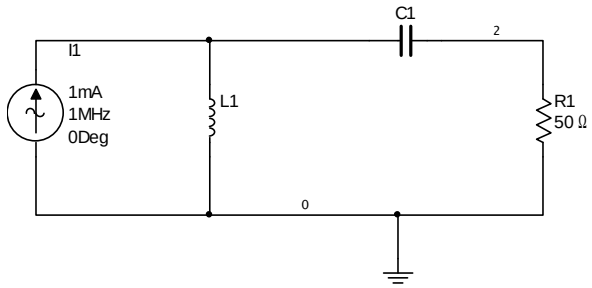


Figure 2- 2 Simple matching network

Since we want to measure the input impedance, we use an ac current source (from the source group, signal current family). We measure the voltage at the input. Set it as shown above. Given that the magnitude of the current is 1 mA, the voltage at the input will give you directly the impedance of the circuit.

* Perform an ac analysis of the circuit. The frequency parameters should be set as follows:

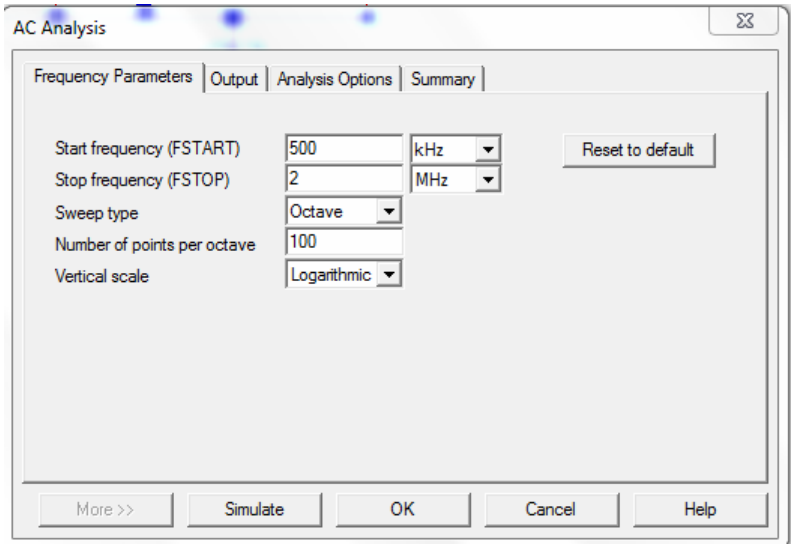


Figure 2- 3 Frequency parameters

* The output node is the common node between the current source, the inductor and the capacitor. Set it using the Output tab. The following figure will appear.

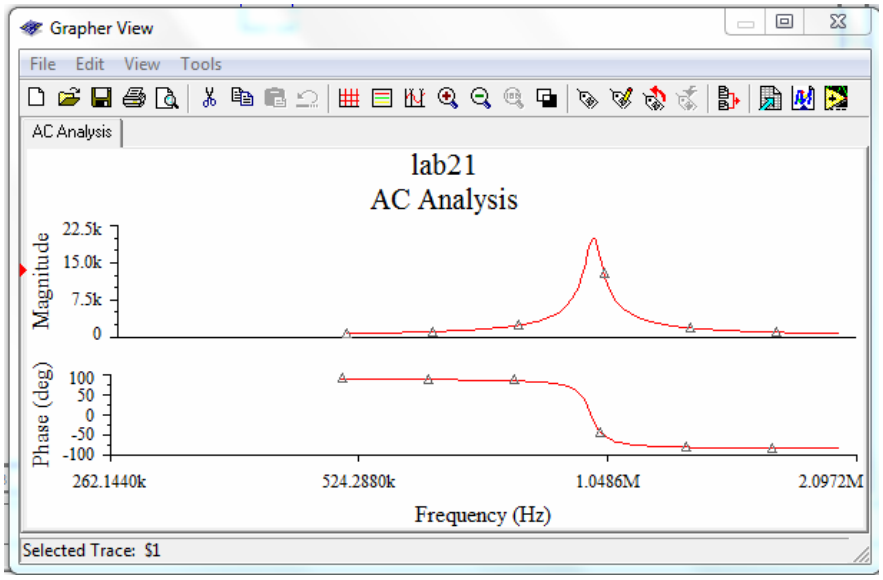


Figure 2- 4 Grapher View

* Select the magnitude trace and press on the cursor button  . Two cursors will appear along with the following window (Figure 2- 5). Use the cursors to measure the impedance at resonance (maximum impedance). Use them also to measure the 3 dB bandwidth.

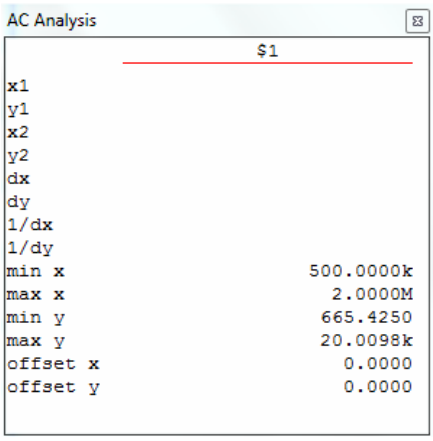


Figure 2- 5 AC Analysis cursor window

One technique for measuring the bandwidth is to determine the frequencies that correspond to a phase response of + and – 45° (Show it). You can move the cursors by right clicking on them. The following window appears:

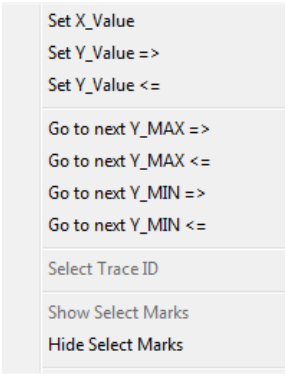


Figure 2- 6 Cursor control window

If you click (left) on Set Y_Value =>, you can move the selected cursor to a position with an ordinate equal to the selected value.

Part 2

In this part, we are going to use a transformer-like network. The selected one uses a split capacitor.

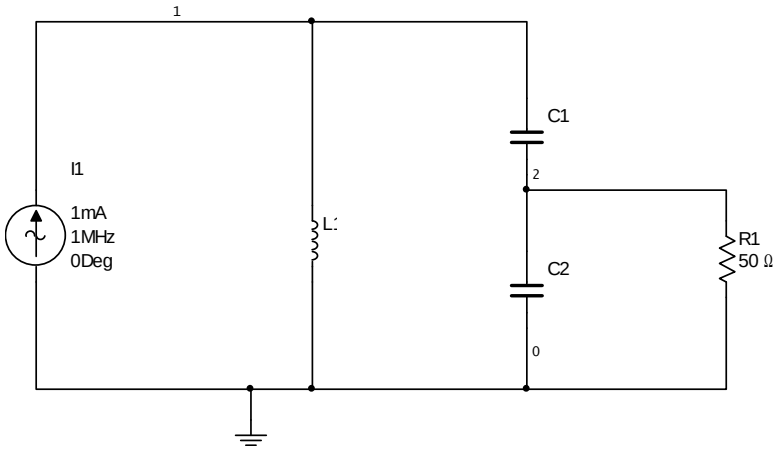


Figure 2- 7 Transformer-like network

For the above network, we add the constraint that the 3dB bandwidth B is 10 kHz. Compute the values of L, C1 and C2. Evaluate $Q_{T'}$, Q_E and n. Does the circuit satisfy the requirements of $nQ_{T'}Q_E \geq 100$ and $Q_E \geq 10$?

* Implement the above circuit.

* Perform an ac analysis of the circuit. The frequency setting in this case should be as follows:

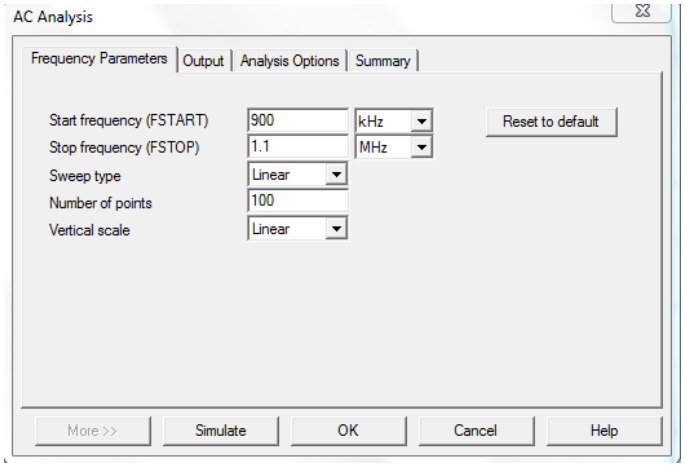


Figure 2- 8 Frequency Parameters

* Measure the value of the impedance at resonance. What is the resonant frequency?

* Use the same technique as in part 1 to evaluate the bandwidth.

* Are your results in accordance with theory?

* Repeat part 2 for the same circuit, but with a 3 dB bandwidth B = 5 kHz.

* Connect a resistance of 20 kΩ in parallel with the inductor. Show that we obtain a bandwidth of 10 kHz with a proper value of $Q_{T'}$, Q_E and n.

* Write an overall conclusion.

Lab 3

Wien Bridge Oscillators

Purpose

The purpose of this set of experiments is to enable the students to the design of typical RC oscillators. The important design parameters (objectives) for this design are:

- The output signal frequency;
- The frequency stability;
- The signal purity (distortion);
- The signal amplitude.

Theory

The Wien bridge oscillator is an RC oscillator characterized by very good frequency stability and very good amplitude stability if it is well designed.

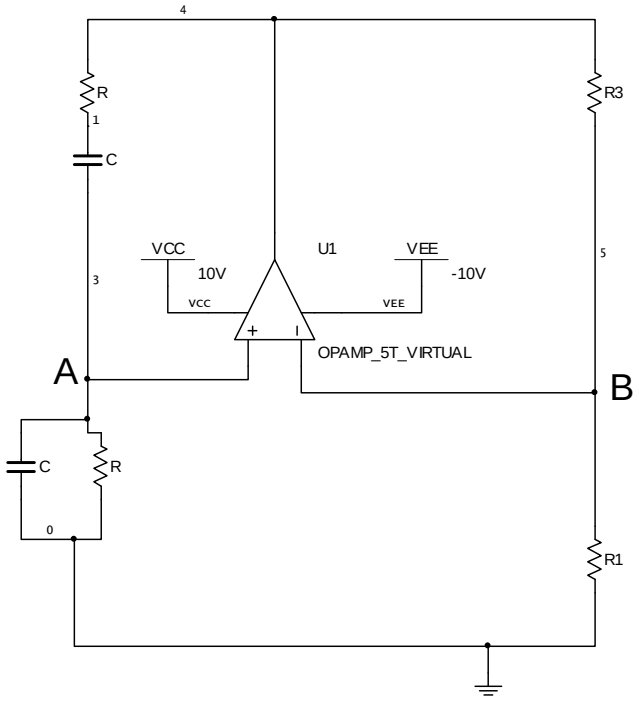


Figure 3- 1 Wien bridge oscillator

From Figure 3- 1, we see that the operational amplifier (op amp) is measuring the difference between the two voltages V_A and V_B and it is connected in such a way that it will try to make that difference as small as possible to bring the bridge to equilibrium.

Question I:

- find the frequency of oscillation and a relation between R1 and R3 when the bridge is at equilibrium ($V_A - V_B = 0$).

The results of question I are valid if and only if the op amp is ideal (infinite gain). A more realistic approach is to consider the amplification as finite. In order to study this system, we will use methods from feedback theory.

Question II:

- find the open loop gain $A_L(s)$ from the following circuit.

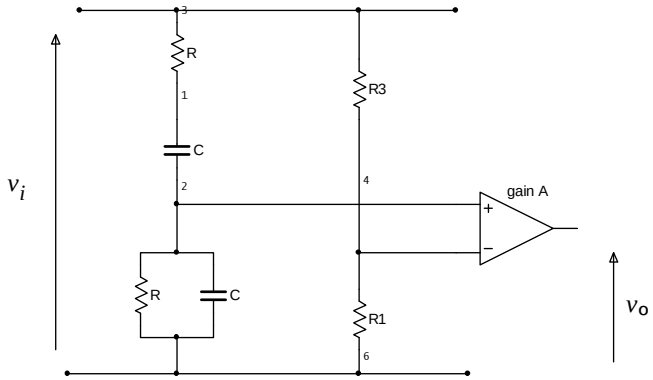


Figure 3- 2 Open loop gain

Use $\omega_0 = \frac{1}{RC}$ and $R3 = (2+\delta)R1$ in order to simplify the expression of $A_L(s)$. You should find:

$$A_L(s) = \frac{-A}{3+\delta}\frac{s^2 - s\delta\omega_0 + \omega_0^2}{s^2 + 3s\omega_0 + \omega_0^2}$$

- Plot its pole and zero diagram.

Question III:

When the output of the op amp is connected to top of the bridge, we obtain a closed loop.

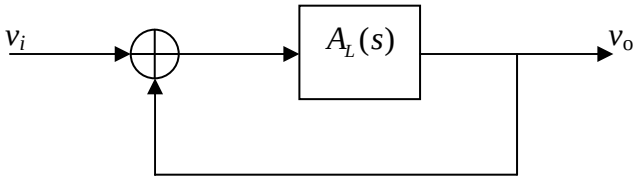


Figure 3- 3 Closed loop

The closed loop gain is given by:

$$G(s) = \frac{v_o(s)}{v_i(s)} = \frac{A_L(s)}{1 - A_L(s)}$$

We can remark that, since $A_L(s)$ is a ratio of two polynomials:

$$A_L(s) = \frac{-A}{3+\delta}\frac{N(s)}{D(s)}$$

The poles of the closed loop transfer function $G(s)$ are given by the following equation:

$$1 - A_L(s) = 0 \text{ or } D(s) + \frac{A}{3+\delta}N(s) = 0$$

So, when the gain of the op amp is very small, the closed loop poles are the same as those of the open loop transfer function $A_L(s)$. When the gain is very large (the usual case), they move toward the zeroes of $A_L(s)$.

The location of the poles of $G(s)$ for different values of the gain *A* is called the "*root locus*" of the system. The system is a sinusoidal oscillator if and only if there is only one pair of closed loop poles on the $j\omega$ axis. The other closed loop poles (if they exist) must be stable. In our case, there is only one pair. If they are on the left half of the *s*-plane, the system is stable and oscillations will not start. If they are on the right half, we will have exponentially growing oscillations that will bring the system to nonlinear operation.

- Find the gain A_0 necessary to have pure imaginary poles. What is their frequency (imaginary part)?

You should find: $A_0 = \frac{9}{\delta} + 3$

- What is the pole location when $A < A_0$ and when $A > A_0$?

We define an "*indirect frequency stability*" coefficient S_F as:

$$S_F = \omega_0 \left.\frac{d\phi}{d\omega}\right|_{\omega=\omega_0}$$

where ϕ is the phase (argument) of the open loop gain $A_L(s)\big|_{s=j\omega}$. In the case of the Wien bridge oscillator, this stability coefficient is given by:

$$S_F = -\frac{2\sqrt{\omega_1\omega_2}}{\omega_1+\omega_2} - 2Q_{Tz}$$

where $-\omega_1$ and $-\omega_2$ are the two poles of $A_L(s)$ and Q_{Tz} is the "Q" of the zeroes:

$$Q_{Tz} = \frac{1}{\delta}$$

Practical part

1. Oscillator without automatic gain control (AGC)

a) Design:

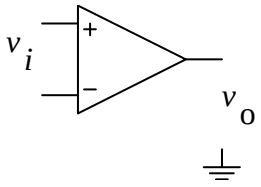
* Compute S_F for δ=1 (R3 = 3R1).

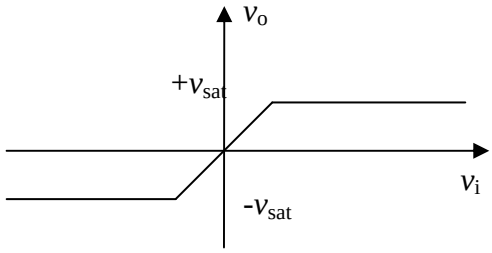
* What is the necessary gain A_0?

* The op amp used in this experiment is the OPAMP_5T_VIRTUAL from the analog group, ANALOG_VIRTUAL family. Its differential gain is 200 000, which is very large. For this case, find the closed loop pole location

* Will this system be a "good" oscillator?

The op amp characteristic is roughly piecewise linear.





* In this case, for the pole location that you have found, would the output be sinusoidal?

* What will be the output amplitude?

* Give an estimate of the output frequency.

b) Implementation:

* Implement the Wien bridge according to Figure 3- 1 with an oscillation frequency $f_0 = \frac{\omega_0}{2\pi} = 1\,\text{kHz}$, δ= 1. Set R = 1 kΩ. The other two resistors should be selected in the ten kΩ range. For this part, use values from the E24 series.

* Connect an oscilloscope and a frequency meter at the output of the op amp.

* Sketch the output waveform.

* Measure its frequency.

* Use the distortion meter, set its frequency at the value measured by the frequency meter and measure the waveform distortion.

2. AGC using FET transistor

a) Design:

The previous design gave a very unsatisfactory oscillator due to the large value of δ. The only way to have a good and very stable oscillator is to choose δ as small as possible.

However, from the equation $A_0 = \frac{9}{\delta} + 3$, we see that if $\delta = 0$, then we need an infinite gain in order to have an oscillation. Since all op amps have very large but finite gain, this condition is impossible to achieve. This means that a Wien bridge oscillator design with $\delta = 0$ (R3 = 2R1) cannot work.

General rule for sinusoidal oscillator design:

- Design the oscillator such that the oscillations always occur at start up (when we turn the power supply on): *Set the closed loop poles at the right of the $j\omega$ axis.* At start up, we will have growing oscillations.
- For some selected amplitude of the output waveform, your design should reduce the gain so that the poles move toward the left of the *s*-plane.

We see that we need some kind of automatic gain control in all sinusoidal oscillators.

In the case of the Wien bridge designed around an op amp, the gain of the amplifier is fixed (if we do not allow the amplitude of the output to reach saturation). However, the condition $A_0 = \frac{9}{\delta} + 3$ shows that we can act on the value of δ in order to have an automatic gain control.

A_0 being fixed, if $\delta > 0$ (but very small), we will have growing oscillations at start up. If we make $\delta < 0$, the closed loop poles will move to the left of the $j\omega$ axis, the amplitude of the oscillation will decay.

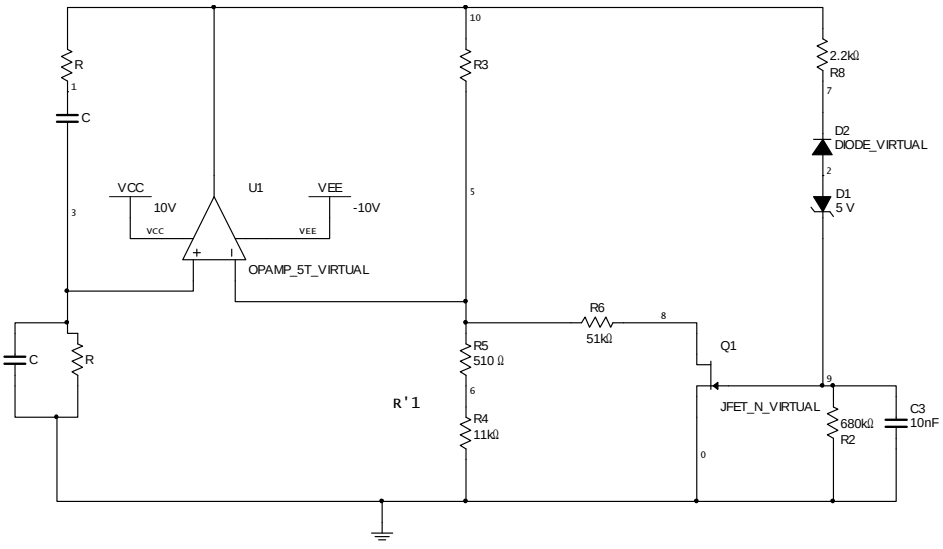


Figure 3- 4 AGC using FET

Using the above defined principle, we are going to make the resistance *R*1 of Figure 3- 1 variable with the output amplitude. In the above figure (Figure 3- 4), the resistance *R*'1 is the

sum of the two resistances $R4$ and $R5$. The resistance $R1$ is the parallel connection of $R'1$ and the series connection of R6 and R_{DS}, $R1 = R'1//(R6 + R_{DS})$. R_{DS} is the resistance of the channel of the FET. If the drain to source voltage is limited to a few hundreds of millivolts, this resistance is given by the following expression:

$$R_{DS} = \frac{V_p^2}{2I_{DSS}\left(\left|V_p\right| + v_{GS}\right)} \qquad V_p \le v_{GS} \le 0$$

The advantage of this method of amplitude stabilization is its low distortion due to the gradual variation of $R1$.

* Explain in a few lines the principle of this method of amplitude stabilization.

In order to simplify the different expressions, let us call $R0 = R3/2$.

* Draw the curve of R_{DS} versus v_{GS} (use $V_p = -2$ V and $I_{DSS} = 0.4$ mA).

In order to minimize the voltage across the channel of the FET, we select $R6$ to be quite large ($R6 = 10R0$).

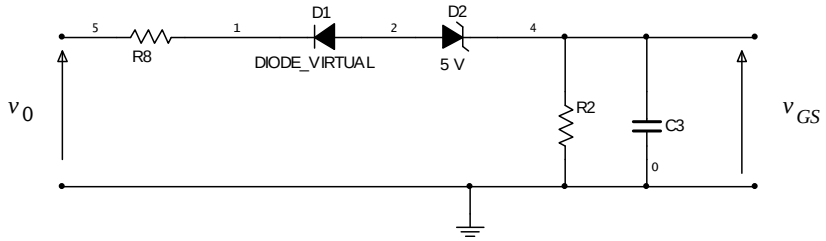
* At start up, C3 is discharged and $v_{GS} = 0$. In this case, we would like to have growing oscillations ($\delta > 0$). What relation should $R'1$ satisfy?

* The amplitude of the output increases. At some point, the Zener diode turns on. The value of R_{DS} will change until the relation $A_0 = \frac{9}{\delta} + 3$ is satisfied. Since A_0 is very large, this relation is satisfied by a very small value of δ. We can safely assume $\delta = 0$. So, $R1 = R'1//\left(R6 + R_{DS}\right) \approx R0$. What is the value of R_{DS} when we have equality?

* In order to have the previous relation satisfied, we must have: $R'1 > R0$.

* With the two inequalities select an appropriate value for $R'1$ as a function of $R0$ ($R'1 = kR0$). Select k.

The circuit at the input of the FET is a peak detector.



* The time constant $R2C3$ must be much larger than the period of the oscillation. The transfer between the voltage v_{GS} and the output amplitude V_0 ($v_0(t) = V_0 \cos \omega_0 t$) is then a piecewise linear characteristic. Make a plot of it.

* The resistor R8 is used to limit the current flowing in the above circuit.

* Design a Wien bridge with FET AGC and f_0 = 1 kHz, $R0$ = 11 kΩ.

* Predict the output amplitude from the two curves you have drawn.

b) Implementation:

* Implement the circuit of Figure 3- 4.

* Visualize the output waveform on the oscilloscope.

* Measure the output frequency.

* Measure its distortion.

* Change the power supply values (double click on VCC and VEE) to + and – 15 V. Do your measurements change?

* Write an overall conclusion.

Lab 4

LC Oscillators

Purpose

The purpose of this set of experiments is to enable the students to design practical high frequency oscillators. The design objectives are the same as for the RC oscillators. We want to build oscillators with:

- Stable frequency
- Stable output amplitude
- Low distortion sinewave.

Theory

Sinewave oscillators operating from few hundreds of kilohertz to few hundred of megahertz are usually designed around a high Q parallel RLC network. The circuit will always produce a sinusoidal voltage even if the driving current is not sinusoidal. When we use LC oscillators, we don't have to perform a complete analysis using the Barkhausen conditions. We know that the phase shift introduced by the network is zero at the frequency of resonance and that the value of the impedance is equal to R. In order to make a small signal analysis (linear case), let us consider the following circuit:

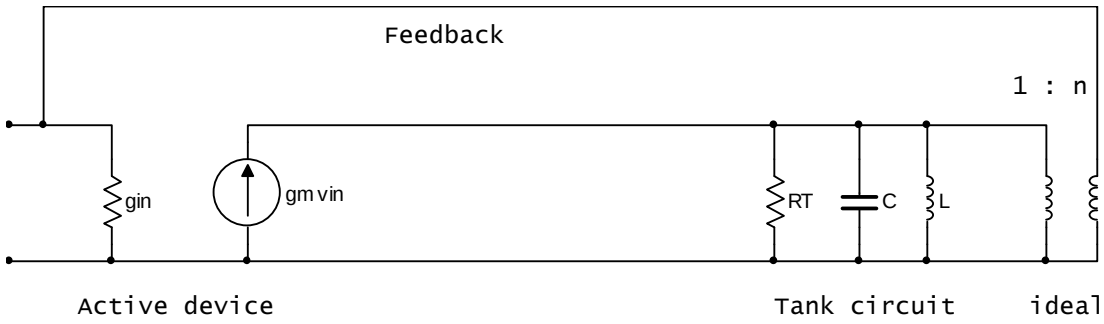


Figure 4- 1 Basic LC oscillator

We can remark that, in the equivalent circuit of the active device, we neglect the effect of all parasitic capacitances. This means that the methods of design that we will demonstrate are valid if and only if we can consider the transistor as memoriless. Furthermore, in order to neglect the effect of the output capacitance of the transistor, we should select the tuning capacitance *C* very large compared with it. In order to neglect the effect of the input capacitance and minimize the loading of the tank circuit, we should have the turn ration *n* much less than one. Explain.

Question 1:

* Compute the open loop gain $A_L(s) = \frac{v_0(s)}{v_i(s)}$. The open loop is derived by cutting the feedback path. In our case, it is convenient to cut the path in the middle of the active device. This gives the following circuit:

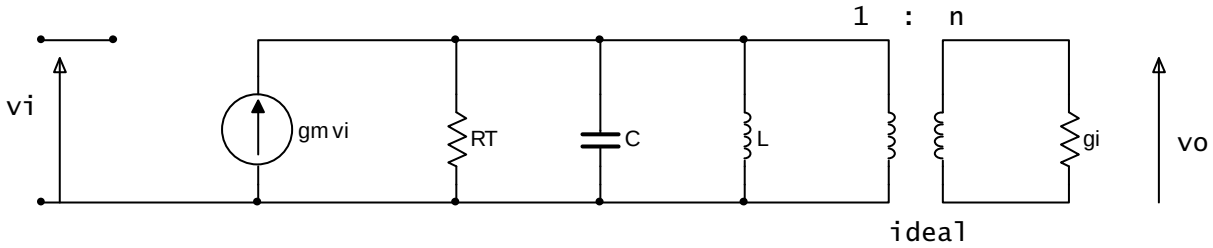


Figure 4- 2 Open loop

* Plot its pole and zero location in the s-plane.

Question 2:

- What is the root locus of the system?

- Determine the minimum transconductance necessary to have closed loop poles on the $j\omega$ axis (g_m minimum).

The previously made analysis is valid for small signals. Using a linear analysis does not predict the amplitude of oscillation. Using linear methods, we know that the amplitude of the response of a dynamic system depends only on initial conditions which are impossible to predict. Furthermore, we need an infinite precision in the evaluation of g_m in order to put a pair of closed loop poles on the $j\omega$ axis.

If g_m is smaller than g_m minimum, the oscillations will not start.

If g_m is larger than g_m minimum, the oscillations will start (exponentially increasing) and the amplitude of the oscillation is determined by the inherent nonlinearities of the active device used in the circuit. These nonlinearities will reduce the gain of the active device and will move the closed loop poles to the imaginary axis.

We need a large signal analysis in order to determine the amplitude and the distortion of the output signal.

Practical part

BJT common base Colpitts oscillator

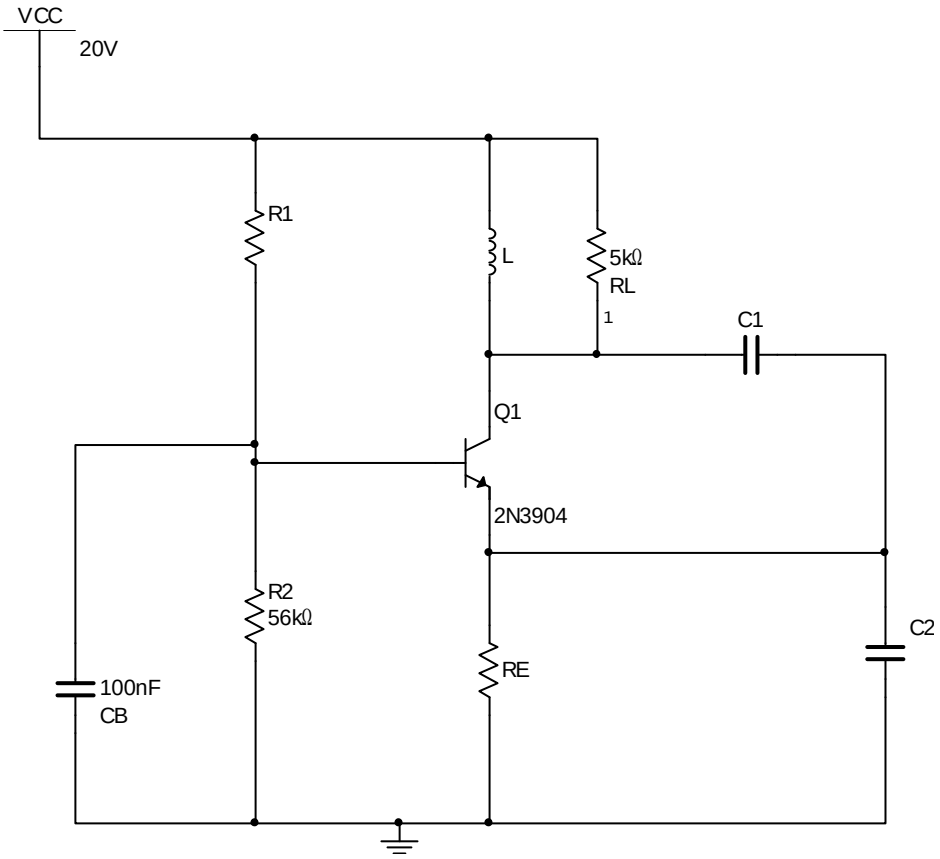


Figure 4- 3 Common base Colpitts oscillator

We want to design an oscillator that delivers an output voltage of 4 V peak to a load RL of 5 kΩ at a frequency of 1 MHz. For general oscillators, we have to make he study in two steps. The small signal analysis is used for the analysis of the start up conditions and the large signal analysis is used for determining the amplitude of the waveform.

For the small signal analysis, we use the following model for the active device:

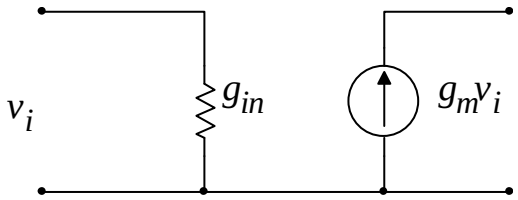


Figure 4- 4 Small signal model

In the above model, we have: $g_{in} = \frac{qI_{EQ}}{kT}$ and $g_m = \frac{qI_{CQ}}{kT} = \alpha g_{in} \approx g_{in}$.

Step 1: Small signal analysis.

The equivalent circuit is:

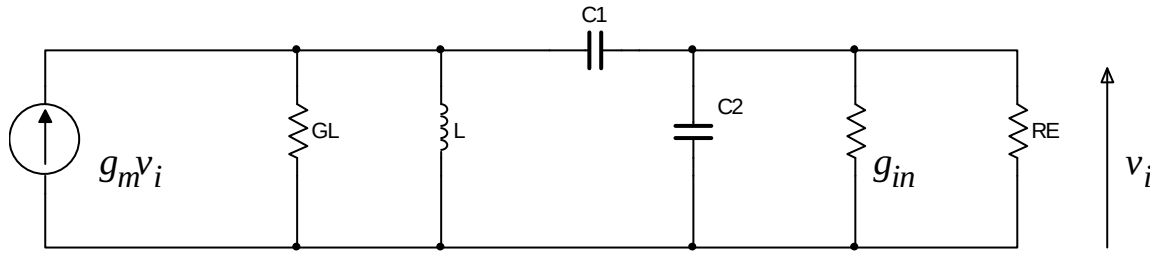


Figure 4- 5 AC equivalent circuit

In general, the value of the emitter biasing resistance (RE) is much larger than the input resistance of the common base circuit $r_{in} = 1/g_{in}$. So, we can neglect its effect on the circuit.

If we make a given number of assumptions, we can transform the above circuit into the following shape:

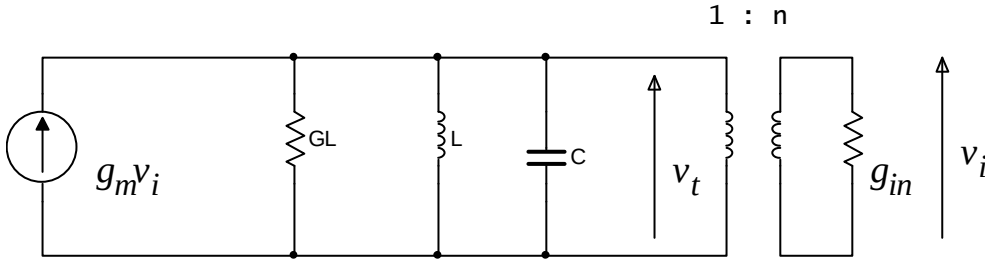


Figure 4- 6 Small signal equivalent circuit

* State whatever assumptions you have made.

* What is the frequency of oscillation?

* Show that, in order to start the oscillations at a given frequency ω_0, we must have:

$$g_m > g_{m\,\min} = \frac{G_L}{n\left(1-\frac{n}{\alpha}\right)}$$

So, your design should fix $g_m = \alpha \frac{qI_{EQ}}{kT}$ to a value larger than $g_{m\,\min}$ for the oscillations to start (see previous lab experiment). However, this value should not be too large because we have seen in lab #3 that in this case, we will have too much distortion and the frequency will be lower than the one desired. In some cases, if the gain is too large, the closed loop poles will move to the real axis (positive) and the oscillations will not occur.

* If the biasing is set such that the above condition is satisfied, what will the evolution of the oscillations be?

Step 2: Large signal analysis.

We are going to use the transistor nonlinearity to stabilize the amplitude. We have studied in the course that the large signal transconductance of the transistor decreases with increasing amplitude. So, at start up, since the gain is set so that the closed loop poles are on the right side of the imaginary axis, we will have growing oscillations (the system favors only one frequency). At start up, the gain is set by the small signal transconductance. As the amplitude increases, the gain decreases until we reach an equilibrium value.

For the large signal analysis, we don't have to do a complete analysis. The only frequency for which the total phase shift of the open loop is zero is the resonant frequency of the tank circuit. So, we know that the oscillation will occur at the frequency $\omega_0 = 1/\sqrt{LC}$. Another point worth noting is that the tank circuit is going to filter the current and the voltage across the parallel RLC circuit is going to be sinusoidal. This also entails that the voltage applied across the base emitter junction will be the sum of a sinewave and a dc voltage ($Q_T > 10$)

The voltage applied at the base emitter junction is sinusoidal, the current i_E is not. However, the only component that will have an effect (loading the tank circuit) is the fundamental. It is shown in the textbook (pp.188-190) that this load has the same effect as a conductance of value $G_{NL} = G_m(x)/\alpha$. So, if we consider only the fundamental current, the equivalent circuit for large signals is:

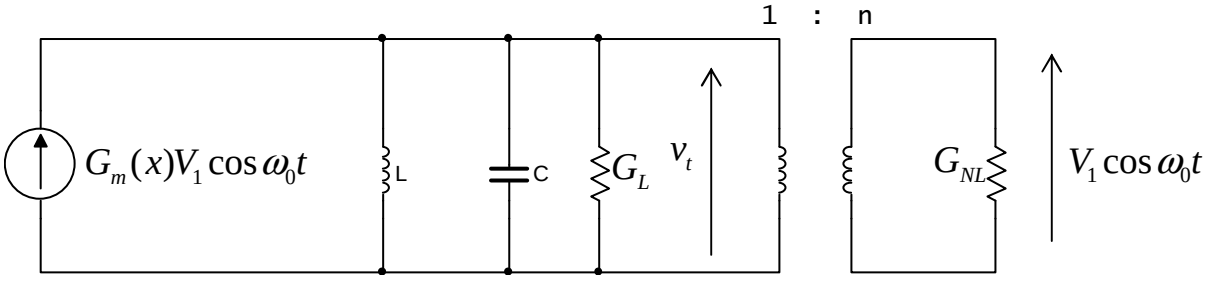


Figure 4- 7 Large signal equivalent circuit

* What is the condition that must be satisfied by $G_m(x)$ in order to have stable oscillations (closed loop poles on the $j\omega$ axis)?

* What is the amplitude of the output?

If we have (as assumed in the theoretical part) $n << 1$, the above condition can be simplified to:

$$\frac{G_m(x)}{g_m} = \frac{G_L}{ng_m}$$

In order to have stable oscillations, we should have *x* as large as possible. However, in this case, the distortion will be very large also. Once the value of *x* is fixed, the ratio $\frac{G_m(x)}{g_m}$ can be read from the appropriate curve (from the textbook or your course notes). The amplitude of the ac signal $v_t = V_t \cos \omega_0 t$ at the collector is $V_t = 4\ \text{V}$.

Design

Let *x* = 10 (this is a reasonable value that does not produce too much distortion and provides a good amplitude stability). Find V_1 and $\frac{G_m(x)}{g_m}$.

Since $V_1 = n\, V_t$, *n* is given.

We assume that the total *Q* of the tank circuit is given by $Q = R_T C \omega_0$. What did we neglect? We fix its value at $Q = 20\pi \approx 62.8$.

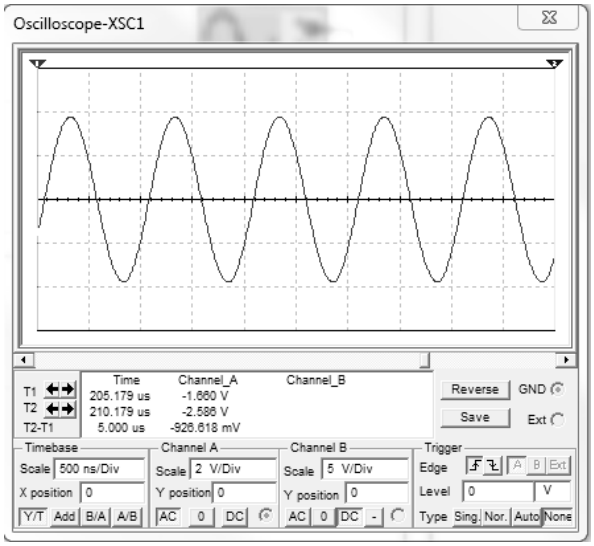
Compute *C*, *L*, C_1, C_2 and g_m.

The value of g_m fixes the biasing current I_{EQ}. Since we want a quite small output as compared with the power supply ($V_t = 4\ \text{V}$, VCC = 20 V), we can select a large voltage for $V_\lambda = R_E I_{EQ}$). Let $V_\lambda = 9.35\ \text{V}$. Compute the resistances R_E, R_1, R_2.

Verify that all your assumptions are correct.

Implementation

Implement the circuit on Multisim. Use the oscilloscope to observe the output wave form. The oscilloscope setting should be as follows:



* Wait at least 500 µs of simulation time (can be read at the T1 marker of the oscilloscope) before starting the measurements.

*Measure the output amplitude. Is it smaller or larger than the design value of 4 V peak? What element(s) should be adjusted in order to have the proper output of 4 V? Do the adjustment.

* Use the frequency meter to measure the output frequency. Connect the distortion analyzer at the output. Set its frequency to the one measured by the frequency meter. Measure the distortion of the waveform.

* Write an overall conclusion.