

K-Band Two Stages Low Noise Amplifier Design in Microstrip Technology

M. CHALLAL^{1,2}, A. AZRAR¹ and D. VANHOENACKER JANVIER²

¹ Signals and Systems Laboratory, Institute of Electrical Engineering and Electronics, IGEE, University of Boumerdes, UMBB, Boumerdes, ALGERIA.

² Electromagnetics MICrowave Communication laboratory, EMIC, Université Catholique de Louvain la Neuve, UCL, Louvain-La-Neuve, BELGIUM
 mchallal@ieec.org

ABSTRACT

The design of two stages low noise amplifier (LNA) in microstrip technology using active bias networks for K-Band applications is described in this paper. The complete LNA achieves an excellent noise figure of 1.78 dB, a power gain of 15.37 dB with respectively 17.34 dB and 22.33 dB input and output return losses. The simulated results have been compared with measurements reported in the literature and show a good agreement.

Index Terms— Low Noise Amplifier (LNA); Gain; Noise Figure (NF). Matching Network (MN).

1. INTRODUCTION

In most of the microwave and wireless communication RF front end receivers, low noise amplifier (LNA) is the first bloc which amplifies the received RF signal from antenna and provides gain as high as possible with the lowest noise figure possible. The first stage of the amplifier is designed to drive the noise figure and the next stage offers necessary gain. The design procedure is simulated and optimized using the Advanced Design System (ADS) software of Agilent Technologies Inc. The operating frequency of the design is 24.125 GHz. Substrate used is RO4350B Rogers material with $\epsilon_r = 3.66$, substrate thickness $H = 0.254$ mm, and metal thickness $t = 0.035$ mm. The design employs a high-performance super low noise amplifier N-CHANNEL HJ-FET transistor NE3514S02 manufactured by NEC Technologies [1]. The design contains matching networks with microstrip lines (single stub with minimum lengths) and standard lumped elements for the active bias network based on BCR400W. The two stages design has been used since a single stage was powerless to meet the gain at the design frequency.

2. LNA CIRCUIT DESIGN

The LNA topology that has been used is a two stage cascaded design with a first amplifier designed to drive the noise figure and the second one to achieve required gain at desired noise figure as shown in Figure 1. The two stages LNA are based on input, inter-stage and output matching networks abbreviated respectively by IMN, INMN and OMN. BN1 and BN2 are respectively the 1st and the 2nd bias networks.

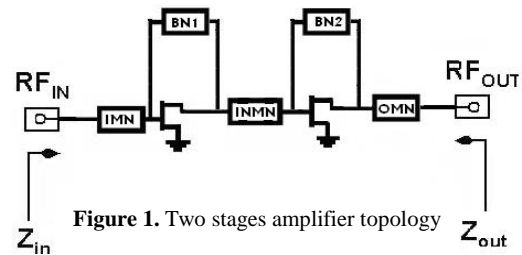


Figure 1. Two stages amplifier topology

The methodology procedure of the LNA design described in [2] is used with taking in consideration stability, gain, noise figure and DC supplies [3-5]. The LNA requirements are shown in the following table.

Table 1. LNA requirements

Parameters	Specifications
Operating frequency [GHz]	24.125
Bias point	V _{ds} = 2 V & I _{ds} = 10 mA
Technology	Microstrip
Gain[dB]	> 15
Noise figure [dB]	< 2
Return loss [dB]	>10
Nbre of stage	02 maximum

Once choosing a DC bias point for the desired gain and noise figure (NF), stability of transistor should be analyzed. Since NE3514S02 is unstable, shunt resistor with 200 ohms is added in the output port. After checking the stability, matching networks (MN) have been considered.

Table 2. Comparison with other reported designs

Ref.	f ₀ [GHz]	V _{ds} / I _{ds} [V]/[mA]	Gain [dB]	NF [dB]	S ₁₁ [dB]	S ₂₂ [dB]
[10]	16	1.5 / 10	10.5	1.82	NA	NA
[11]	22-24	2.5 / 13.8	~ 5	NA	-7 to -2.3	NA
This work	24.125	2 / 10	8.01	1.78	-31	-23

Among different types of MN, there are [6-8]:

- 2.1.1. Lumped Elements
- 2.1.2. Quarter-wave transformers
- 2.1.3. Microstrip line & single (or double) stub
- 2.1.4. Multi-section transformers

For the LNA, MN has been designed on smith chart using single open stub matching technique. When the stub's length and position are properly chosen, the input impedance Z_{in} , seen at the junction of the microstrip stub and the line matches exactly the characteristic impedance Z_o of the system.

The input impedance Z_{in} of a lossless, terminated transmission line is given by [9]:

$$Z_{in} = Z_o \frac{Z_L + jZ_o \tan \beta l}{Z_o + jZ_L \tan \beta l} \quad (1)$$

where Z_L is the terminating impedance, l is the physical distance along the line from the load and β is the phase constant.

In the single stage design, only INM and OMN are to be designed while in the multistage, INMN is also required. The lengths and widths for the microstrip line and stub of the MN are designed using smith chart tool and then further optimized for improved performance. The physical dimensions of these microstrip stubs and lines are calculated with LineCalc tool available in ADS, which based on the properties of the substrate used and the operating frequency.

The performances of the single stage LNA based on NE3514S02 is shown in the following figures. figures 2 and 3 illustrate respectively the Gain and Noise Figure whereas the IRL and ORL versus frequency are shown in figures 4 and 5.

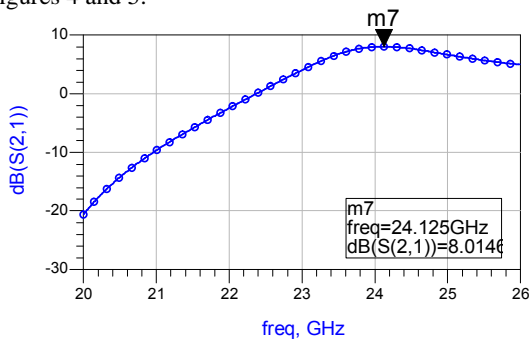


Figure 2. Gain vs. Frequency

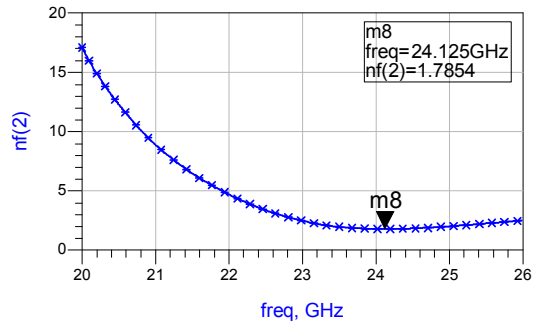


Figure 3. Noise Figure vs. Frequency

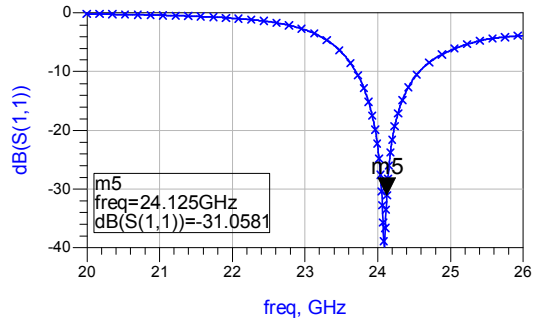


Figure 4. IRL vs. Frequency

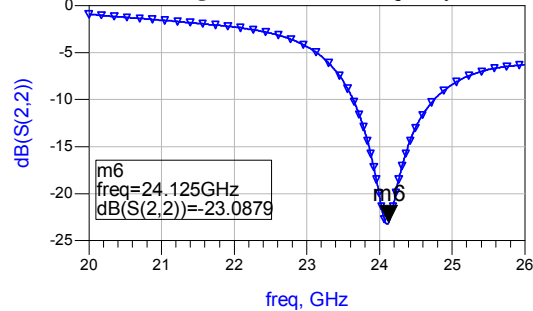


Figure 5. ORL vs. Frequency

The simulated performances are reported in Table 2 together with the measurement presented in other reported designs. Table 2 compares the simulated LNA and the measured parameters reported in the literature. It can be seen that the designed 24 GHz LNA performances compare positively with the different types of technologies used in the state of the art results.

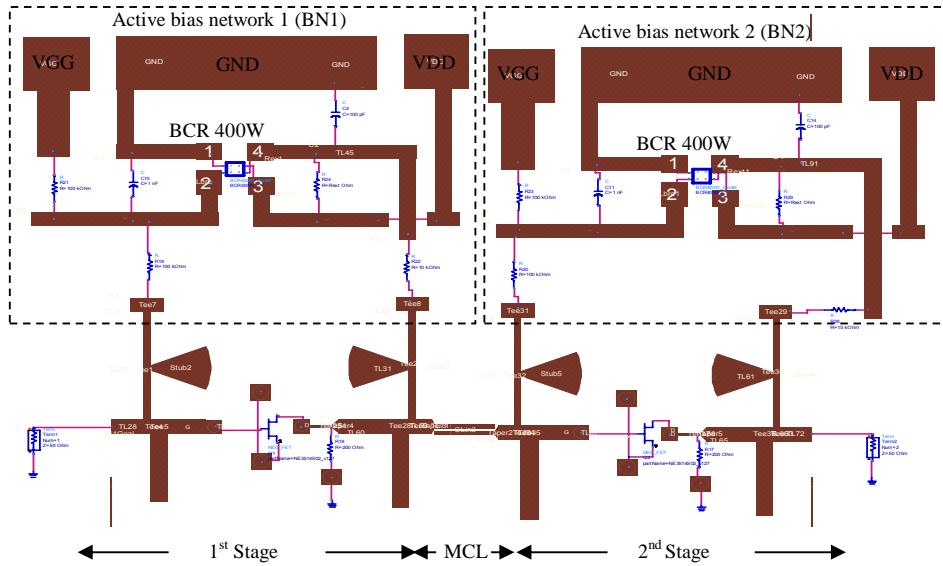


Figure 8. Complete 2 stages LNA layout

To improve the power gain of the designed LNA, a second stage based on the same transistor is added in cascade with the 1st one. In order to isolate the bias between the two stages, microstrip quarter wave coupled line (MCL) is designed and used instead of using capacitor at 24.124 GHz. Figure 6 and Figure 7 show, respectively, the microstrip quarter wave coupled line structure and its performances. The only condition for this structure is that the losses are minimum (or S21) at operating frequency.



Figure 6. Microstrip coupled line

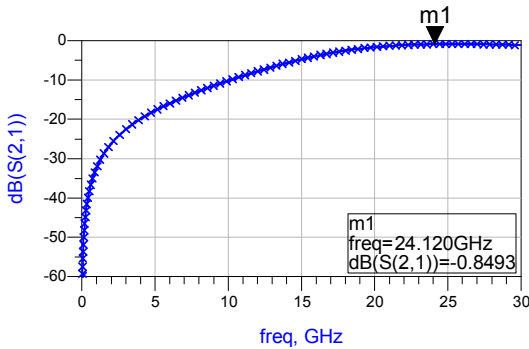


Figure 7. Loss of MCL

For the proposed two stages LNA shown in Figure 8, the simulation results are shown in Figures 9-12. The simulated results show around 24.125 GHz frequency, a gain of 15.37 dB along with 1.78 dB NF, 17.34 dB IRL and 22.33 dB ORL.

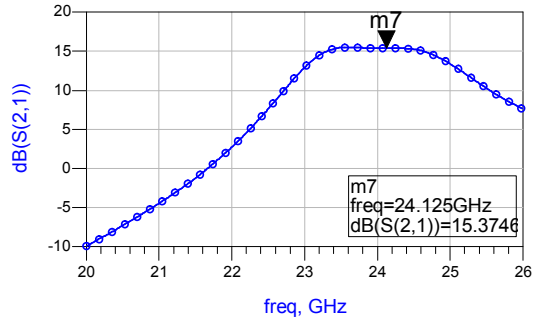


Figure 9. Gain vs. Frequency

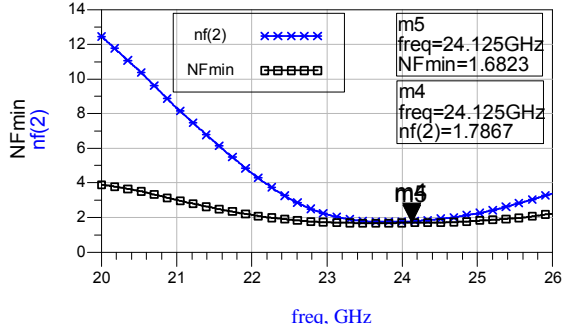


Figure 10. Noise Figure vs. Frequency

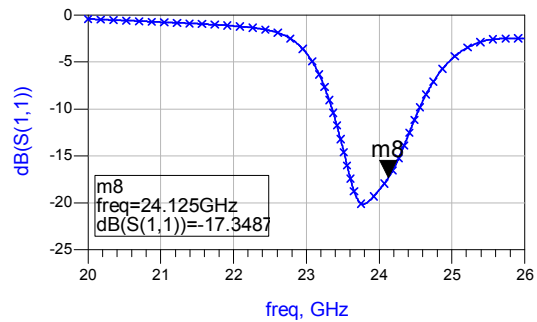


Figure 11. IRL vs. Frequency

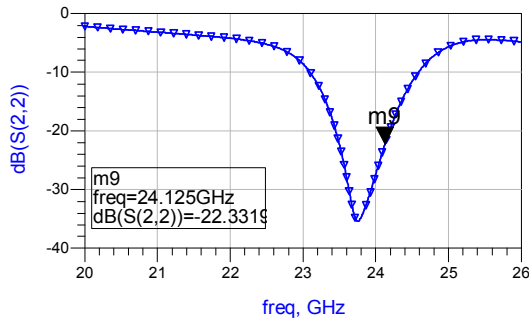


Figure 12. ORL vs. Frequency

The two stages LNA performances summary is shown in Table 3. It can be observed that the simulation results match with the desired requirements and compare positively with reported design.

Table 3. Summary and comparison with other reported design

Ref.	f_0 [GHz]	Vds/Ids [V]/[mA]	Gain [dB]	NF [dB]	S ₁₁ [dB]	S ₂₂ [dB]
[10]	16	1.5 / 10	20.57	1.9	-27	-11.1
This work	24.125	2 / 10	15.37	1.78	-17.3	-22.3

3. CONCLUSION

Two stages low noise amplifier (LNA) in microstrip technology using active bias networks which is modeled in ADS has been designed and simulated. A single stage LNA based on NE3514S02 is designed, simulated and tuned for the best possible gain and noise figure. The simulated results have been compared with measurements reported in the literature and show a good agreement. In order to get a better power gain of the designed LNA, a second stage based on the same transistor is added in cascade with the 1st stage. The design has been adjusted using optimization tools applied on matching networks such that the final design is improved in both gain and noise figure. The complete designed microstrip two stages LNA shows a peak power gain of 15.37 dB, an excellent NF of 1.78 dB, IRL of 17.34 dB and ORL of 22.33 dB under a power consumption of 20 mW.

4. REFERENCES

[1] Nec's Datasheet for NE3514S02 transistor.

[2] M. Challal, A. Azrar, H. Bentarzi and D Vanhoenacker Janvier, "Microstrip Design of Low Noise Amplifier for Application in NarrowBand and WideBand," IEEE 2nd International Conference on Signals, Circuits & Systems, SCS'08, Hammamet, Tunisia, pp. 1-4, November 7-9, 2008.

[3] Pieter L.D. Abrie, "Design of RF and microwave amplifiers and oscillators," Artech House 1999.

[4] G. Gonzalez, "Microwave transistor amplifiers: Analysis and design," 2nd Ed, Prentice Hall, 1997.

[5] Ulrich L. Rohde, David P. Newkirk, "RF/Microwave Circuit design for wireless application," John wiley & sons, Inc. 2000.

[6] Pieter L.D. Abrie, "Design of RF and microwave amplifiers and oscillators," Artech House 1999.

[7] [G.D. Vendelin, A. M. Pavio, U. L. Rohde, "Microwave circuit design using linear and non linear techniques," 2nd Ed, Wiley and Sons, New York 2005.

[8] M. Challal, D. Vanhoenacker Janvier, A. Azrar, H. Bentarzi, A. Reციoui and M. Dehmas, "On Low Noise Amplifier Design for Wireless Communication Systems," Proc. of the IEEE 3rd International Conference on Information & Communication Technologies ICCTA'08, Syria, pp. 725-726, April 2008.

[9] Inder Bahl and Prakash Bhartia, "Microwave Solid State Circuit Design," 2nd Edition, John Wiley & Sons, Inc., Hoboken, New Jersey, 2003.

[10] Tahir Abbas, Mojeeb Bin Ihsan, "Design of a two stage Low Noise Amplifier at Ku band," The 17th International Conference on Microelectronics, ICM 2005, Vol., Issue , pp. 40 - 45, 13-15 Dec. 2005.

[11] Roselli L., Alimenti F., Comez M., Palazzari V., Placentino F., Porzi N., Scarponi A. "A cost driven 24 GHz Doppler radar sensor developpement for automotive applications," Radar conference, EURAD 2005 European, v. 3, pp. 335-338. issue, 6-7 Oct. 2005.