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Two-stage 24 GHz Low Noise Amplifier for Front-End Receiver System

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Abstract: In this paper, two-stage low noise amplifier (LNA) using active bias networks (BCR 400W) operating around 24 GHz for front-end receiver system is described. The designed and optimized LNA by means of ADS software achieves an excellent noise figure of 1.78 dB, a power gain of 15.37 dB with respectively 17.34 dB and 22.33 dB input and output return losses. In order to validate the designed two-stage LNA, the obtained simulation results have been compared with the measurements reported in the literature. The Experimental results agree well with the simulation results.
Key words: Low Noise Amplifier (LNA); Active bias (BCR 400W); Gain; Noise Figure (NF); Return Loss (RL).

INTRODUCTION

Low Noise Amplifiers (LNAs) are key components in the front-end receiver system; they amplify the received RF signal from antenna. Nowadays, a lot of effort has been put into the design of LNA to provide gain as high as possible with lowest noise figure possible and lowest cost of fabrication. Generally, the first stage of the LNA is designed to drive the noise figure and the next stage offers necessary gain.

In this paper, the analyzed and the optimized LNAs for a narrowband application around 24 GHz based on one and then two stages are carried out by the Advanced Design System (ADS) software of Agilent Technologies Inc. The operating frequency of the design is 24.125 GHz and the substrate used is RO4350B Rogers material with relative permittivity and thickness are equal to 3.66 and 0.254 mm respectively. The design employs a high-performance super low noise transistor (NE3514S02) manufactured by NEC Technologies [NEC 06] and it contains matching networks with microstrip lines (single stub with minimum lengths) and standard lumped elements for the active bias network based on BCR 400W. While a single-stage was powerless to meet the gain at the design frequency, the two-stage design has been used.

1. Active bias circuit

The most important purpose of the active bias circuit is to maintain the drain current of the transistor. The S-parameters of the transistor are fixed and do not change as the correct bias current is maintained. A drop in bias current will cause the transistor gain and output power to fall. If more stable bias current is required, an active bias circuit such as the active current mirror, the BCR400, is recommended.

To make a decision if an active bias circuit is appropriate, various important factors should be considered related to its availability in the market, cost and the improvement it provides. The availability of free samples of BCR 400W device is a significant issue to perform the analysis. A BCR 400W is designed for stabilizing bias current from less than 0.2 mA to 200 mA even at low voltage [INF 07]. This circuit is based on two diodes, two resistances and a PNP transistor. The different elements are provided in spice model by Infineon technologies and its application in controlling a transistor is shown in figure 1 [INF 09].

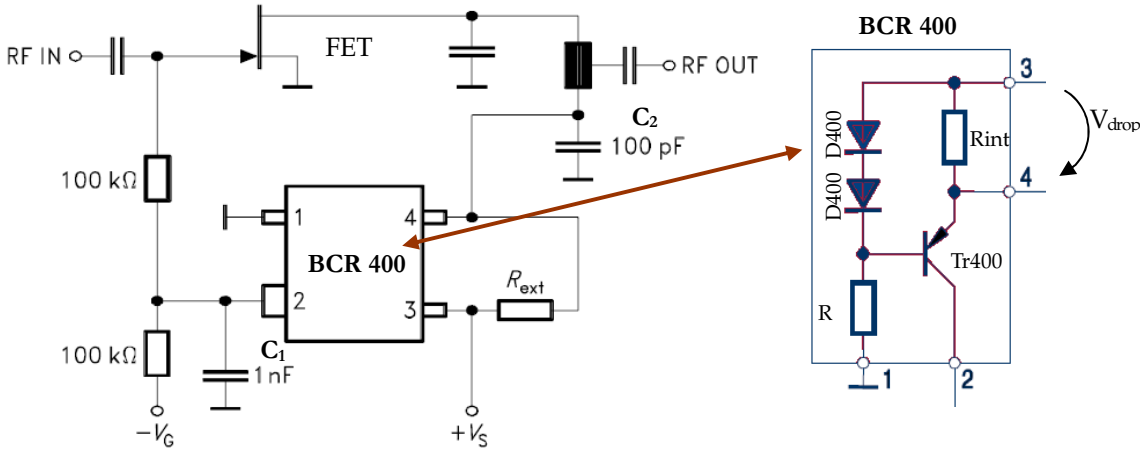

Figure 1. *FET controlled by BCR400 [INF 09]*

The active bias circuit (shown in Figure 1) operates by adjusting both the gate bias voltage (V_G) and the supply voltage (Vs) to maintain a particular value of the drain current (I_D). If current I_D falls then the current flowing through the PNP Tr400 transistor to the negative rail will increase. An increase in the current will cause a larger potential difference across the resistor 100 kΩ to the negative rail. The voltage at the other end of the resistor (connected to the FET gate through another 100 kΩ resistor) will also increase. A more positive voltage on the FET gate (the two diodes become reversed) will causes a larger I_D to flow. Therefore, stabilizing the circuit and preserving a constant current to the FET.

In order to make sure that the modeled BCR 400W operates perfectly, it is applied to bias a transistor as shown in Figure 2 whereas the characteristic curves are illustrated in Figure 3 The I_D versus V_S characteristics for different external resistance Rext values is shown in Figure 3a. It can be observed that, for a fixed value of Rext and when the bias voltage varies from 2 to 10 V, the drain current remains approximately constant (stable). The I_D versus Rext for different Vs values is shown in Figure 3b. It shows that the I_D is inversely proportional to the Rext. Comparing the obtained results to those reported in datasheet [INF 07], the BCR 400W modeled in ADS software works perfectly.

It is observed that Even though an active bias network involve more components and are costly, they present significant and important advantage in maintaining a stable bias current which is very important in LNA circuits.

2. Circuit design

The LNA topology that has been used is a two stage cascaded design with a first amplifier designed to drive the noise figure and the second one to achieve required gain at desired noise figure. The two-stage LNA is based on input, inter-stage and output matching networks abbreviated by IMN, INMN and OMN respectively.

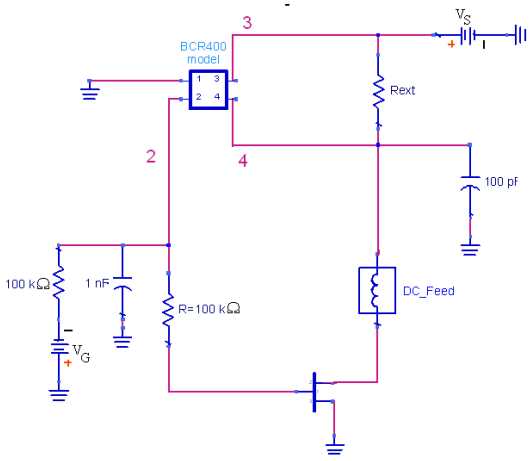

Figure 2. *Electrical schematic of biasing of the transistor by a BCR400W*

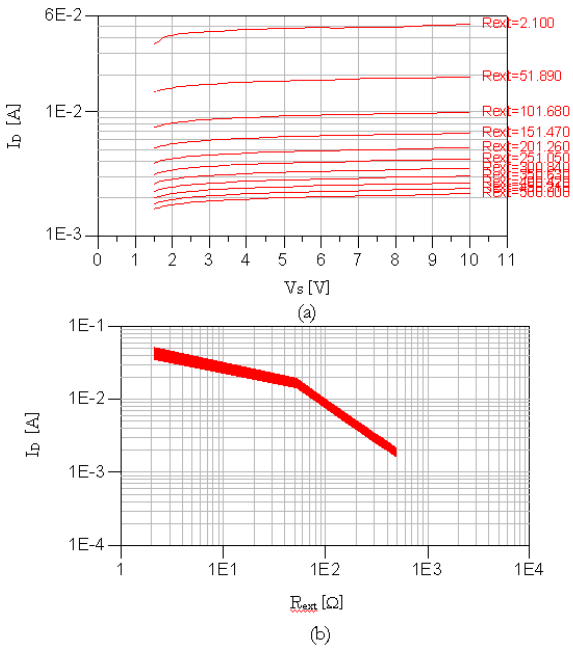

Figure 3. *Characteristic curves of BCR400W (a) ID vs VD and (b) ID vs Rext*

Table 1. *Comparison with other reported designs (0ne-stage LNA)*

Ref.	f_0 [GHz]	Vds/ Ids [V]/[mA]	Gain [dB]	NF [dB]	S_{11} [dB]	S_{22} [dB]
[ROS 05]	22-24	2.5 / 13.8	~ 5	NA	-7 to -2.3	NA
This work	24.125	2 / 10	8.01	1.78	-31	-23

The methodology procedure of the LNA design described in [CHA 08] is used with taking in consideration stability, gain, noise figure and DC supplies [ABR 99 - CHA 08]. The LNA requirements are as following: Operating frequency, Gain, Noise figure, Return loss and Nbre of stage are equal respectively to 24.125 GHz, > 15 dB, < 2 dB, >10 and 02 maximum.

Once choosing a DC bias point for the desired gain and noise figure (NF), stability of transistor should be analyzed. Since NE3514S02 is unstable, shunt resistor with 200 ohms is added in the output port. After checking the stability, matching networks (MN) have been considered.

For the LNA, MN has been designed on smith chart using single open stub matching technique. When the stub's length and position are properly chosen, the input impedance Z_{in}, seen at the junction of the microstrip stub and the line matches exactly the characteristic impedance Z_o of the system.

The input impedance Z_{in} of a lossless, transmission line is given by [BAL 03]:

$$Z_{in} = Z_o \frac{Z_L + jZ_o \tan \beta l}{Z_o + jZ_L \tan \beta l} \qquad (1)$$

where Z_L is the terminating impedance, l is the physical distance along the line from the load and β is the phase constant.

In the single stage design, only INM and OMN are to be designed while in the multistage, INMN is also required. The lengths and widths for the microstrip line and stub of the MN are designed using smith chart tool and then further optimized for improved performance. The physical dimensions of these microstrip stubs and lines are calculated with LineCalc tool available in ADS, which based on the properties of the substrate used and the operating frequency.

The performances of the single stage LNA based on NE3514S02 is shown in the figures 4, 5, 6 and 7.

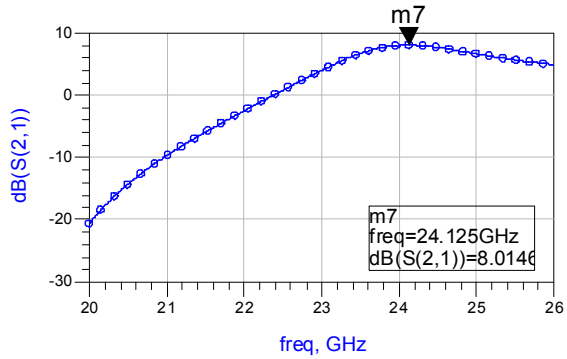

Figure 4. *Gain vs. Frequency*

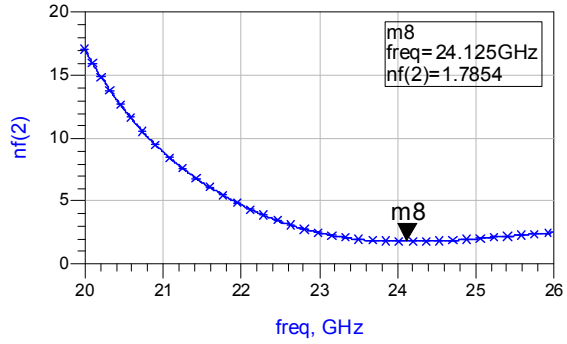

Figure 5. *Noise Figure vs. Frequency*

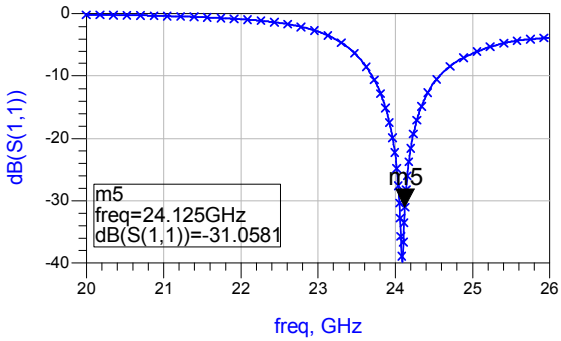

Figure 6.. *IRL vs. Frequency*

Figures 4 and 5 illustrate respectively the Gain and noise figure (NF) whereas the IRL and ORL versus frequency are shown in figures 6 and 7.

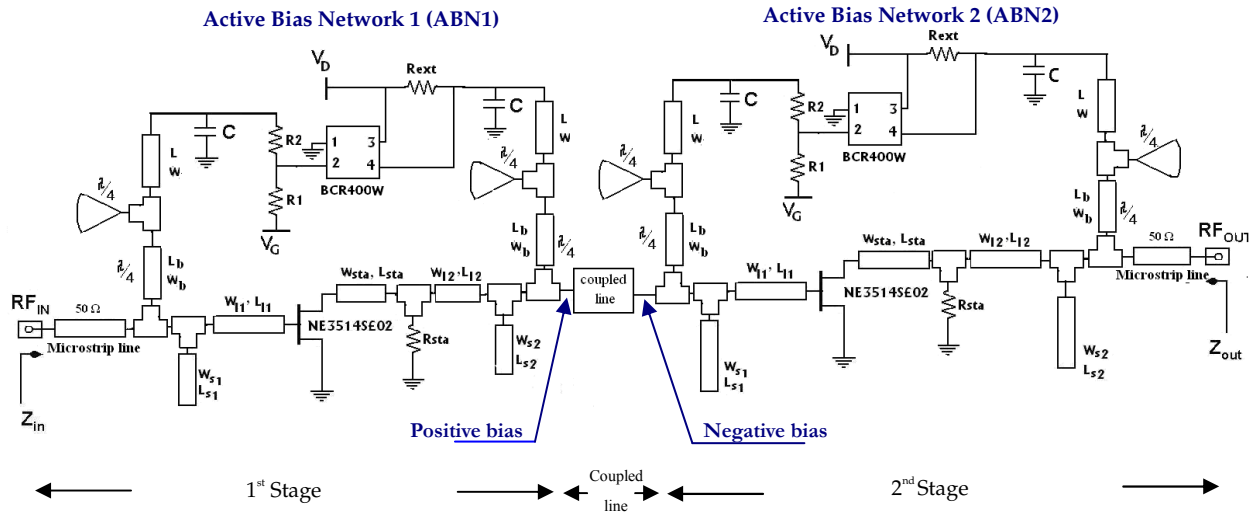

Figure 8. *Electrical schematic of two-stages 24 GHz LNA based on NE3514S02*

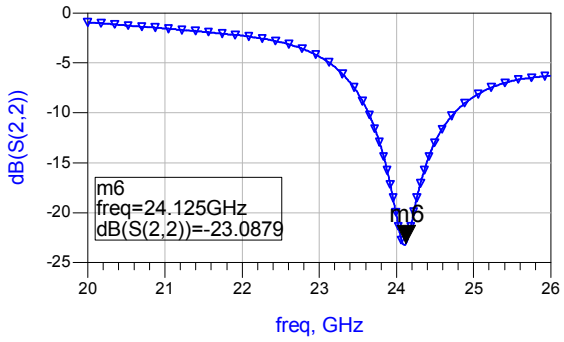

Figure 7. *ORL vs. Frequency*

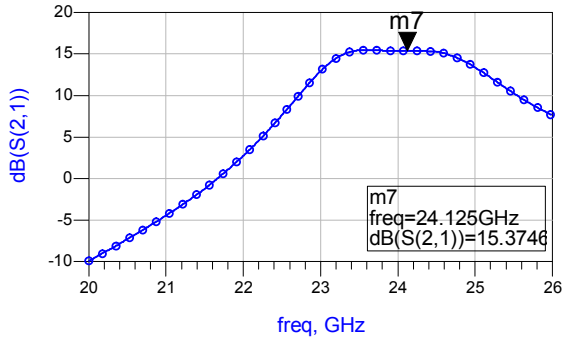

Figure 9. *Gain vs. Frequency*

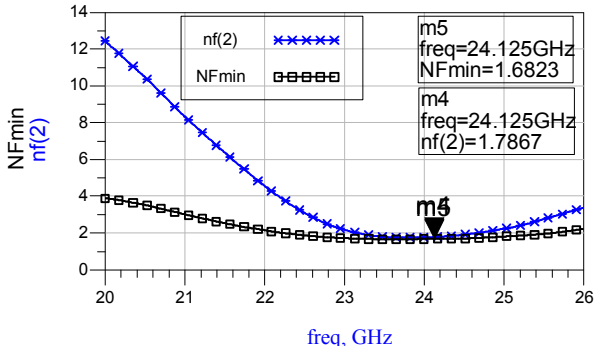

Figure 10. *Noise Figure vs. Frequency*

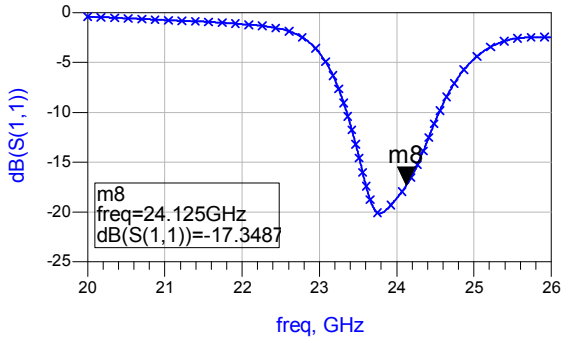

Figure 11. *IRL vs. Frequency*

The simulated performances are reported in Table 1 together with the measurement presented in other reported designs. Table 1 compares the simulated LNA and the measured parameters reported in the literature. It can be seen that the designed 24 GHz LNA performances compare positively with the different types of technologies used in the state of the art results.

To improve the power gain of the designed LNA, a second stage based on the same transistor is added in cascade with the 1st one. In order to isolate the bias between the two stages, microstrip quarter wave coupled line (MCL) is designed and used instead of using capacitor at 24.124 GHz. The only condition for this structure is that the losses are minimum (or S21) at operating frequency.

For the proposed two-stage LNA shown in Figure 8, the simulation results are shown in Figures 9-12. The simulated results show around 24.125 GHz frequency, a gain of 15.37 dB along with 1.78 dB NF, 17.34 dB IRL and 22.33 dB ORL.

Table 2. *Comparison with other reported designs (Two-stage LNA)*

Ref.	f_0 [GHz]	Vds/ Ids [V]/[mA]	Gain [dB]	NF [dB]	S_{11} [dB]	S_{22} [dB]
[Abb05]	16	1.5 / 10	20.57	1.9	-27	-11.1
This work	24.125	2 / 10	15.37	1.78	-17.3	-22.3

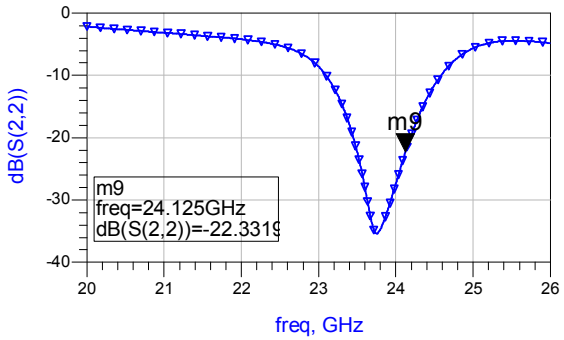

Figure 12. *0RL vs. Frequency*

The two-stage LNA performances summary is shown in Table 2. It has been observed that the simulation results match with the desired requirements.

3. Conclusion

Two-stage low noise amplifier (LNA) operating around 24 GHz for front-end receiver system is designed and optimized. In order to bias the circuit, active bias (BCR400W) networks modeled in ADS have been verified and afterward used. It has been shown that although they involve more components and are costly, they present significant and important advantage in maintaining a stable bias current which is very important in LNA circuits. The designed two-stage LNA shows a peak power gain of 15.37 dB, an excellent NF of 1.78 dB, IRL of 17.34 dB and ORL of 22.33 dB. The simulation results have been compared with the measurements reported in the literature. The measurement results have shown the good agreement with the simulation results.

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