Communication circuits

part 1

EE312

by

A. DAHIMENE

Institut de Génie Electrique et Electronique

Université M'Hamed Bougara
Boumerdes

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Communication circuits

Introduction

This course is about electronic circuits applied to communication. We will deal essentially with C.W. communication. In C.W. communication, we need to produce carriers, amplify band pass signals, and multiply either a band pass signal with a carrier or a baseband signal with a carrier. We will also consider raising the level of a signal in order to either demodulate it or to transmit it. We see that most of the signal processing needs some non linear processors. So, the different electronic devices that we will consider in this course are going to be studied as large signal amplifiers and their behavior will be essentially non linear.

In order to obtain analytically tractable models for the different electronic components, we will assume that they are memoriless. This means that the type of analysis that we will perform in this course is valid at frequencies below the different cut-off frequencies. So, the models will be static and not dynamic.

We assume that the student has a basic knowledge of network analysis and basic electronic devices (diodes, transistors and operational amplifiers). However, we are going to provide a small review of that basic knowledge in the first chapter of the course.

Chapter 1

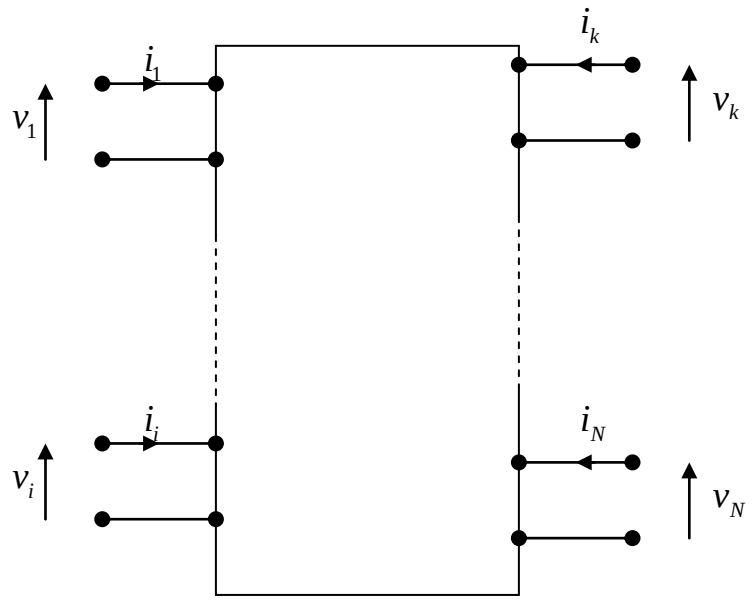
Review of Electronic Devices

1.1 Some Generalities about networks.

The electronic devices that we are going to analyze are essentially non linear active devices. So, we start by defining the notions of linearity and activity in networks.

Linear Network: A network is linear if superposition applies.

Active Network:



Consider the above N port network. The average power dissipated by the network is:

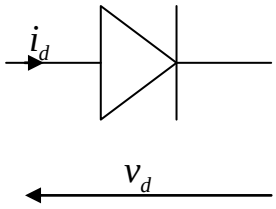
$$P = \langle v_1 i_1 + v_2 i_2 + \cdots + v_N i_N \rangle$$

If $P > 0$, the network dissipates power and should be considered as passive. If $P < 0$, the network provides power to some circuits connected to its ports (it is amplifying power), and at that time the network is active. If $P = 0$, then we say that the network is lossless. Networks built with pure inductors, capacitors and transformers are lossless. In the above representation of the network, we should not include the power supplies as input ports because in that case, all networks

will be passive. This is due to the fact that amplifiers (active devices) transfer power from the power supply to the output port. A device like a diode is a nonlinear one port device, but it is passive. A voltage source will be an active one port device according to the above definition.

1.2 The Diode Model:

The diode is built using a junction of P and N doped semi-conductors. If we apply a voltage across the junction, a current is going to flow though the junction and is composed of two different types of carriers: The majority carriers which compose the diffusion current and the minority carriers that compose the saturation current.



The diode equation is thus: $i_d = I_s \exp\frac{qv_d}{kT} - I_s$ where the first term is the diffusion current which depends mostly on the applied voltage v_d while the saturation current I_s is independent on the applied voltage (as long as v_d is smaller than the avalanche or Zener voltage). The different constants are: q: the electron charge = 1.6 10^{-19} C, k: Boltzman's constant = 1.38 10^{-23} J/°K and T: the temperature in °K. At ambient temperature (T = 300°K), the constant $\frac{kT}{q}$ has the value of 26 mV.

At this point, we should indicate that the electrical field in a reverse biased junction (inside the "depletion region") accelerates the minority carriers.
The following figure shows the forward characteristic of a diode for currents that do not exceed 10 mA.

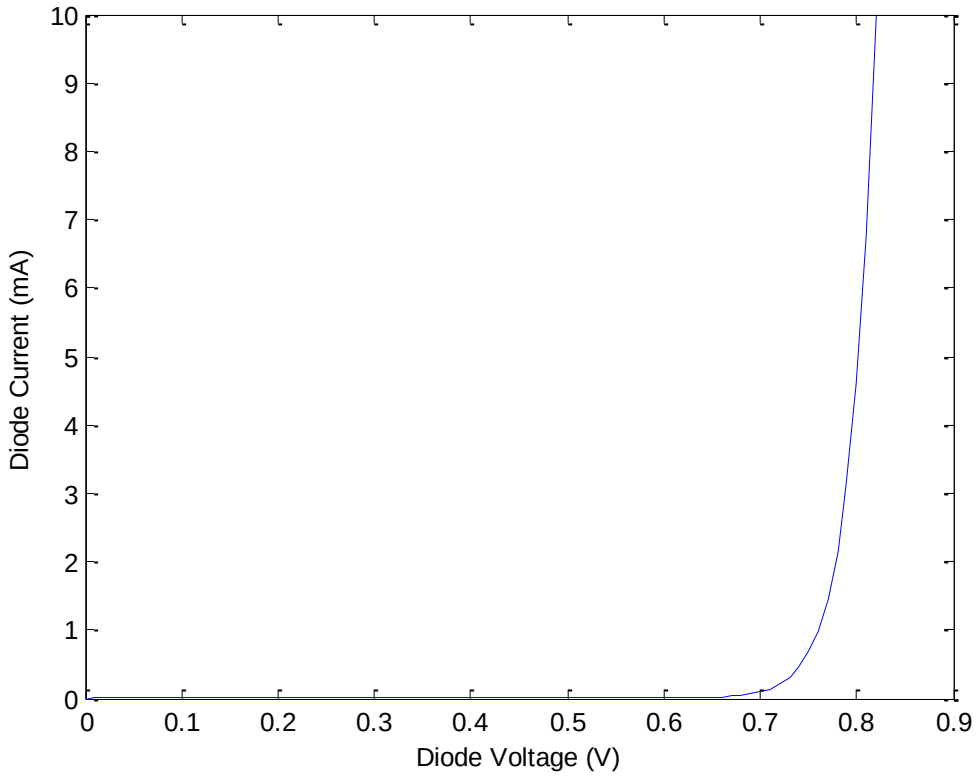
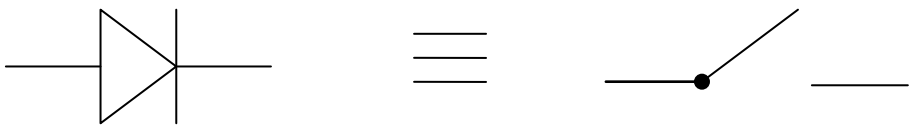


Fig. 1-1 I-V characteristic of a Diode

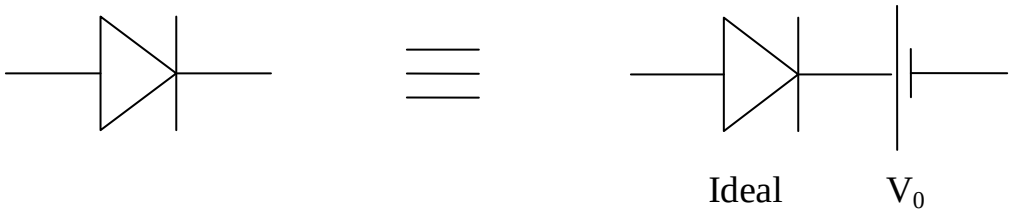
The above figure shows clearly that as long as the voltage is smaller than a threshold V_0, the current is essentially zero, and that above threshold the current is not limited at all. So, a good approximation of the diode is a voltage controlled switch called the "ideal diode" followed by a battery.



ideal

Closed when $v_d>0$

So, finally, a quite simple model (and at the same time fairly accurate) is the following one.

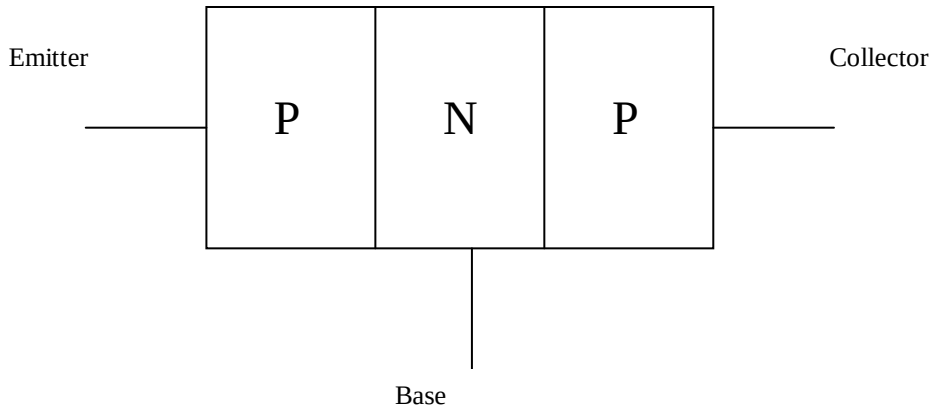


The threshold value will depend on the technology and the type of semi-conductor used. Typical values for V_0 valid for currents between 0.1 to 10 mA are: 0.2 V for Ge, 0.7 V for Si, around 1 V for leds (GaAs, etc) and about 0.4 V for Schottky diodes. Depending on the problem at hand, we will use one of the different models seen above.

The exponential model will be used to model the Bipolar Junction transistor (BJT).

1.3 The Bipolar Junction Transistor:

Consider a piece of silicon with three areas that will form two PN junctions.



Let the base-emitter (BE) junction be forward biased and the collector-base (CB) junction be reverse biased. At that time, a majority carrier injected at the

emitter (a hole going from emitter to base or an electron going from base to emitter) is going to find itself inside the depletion region of the reverse biased collector base junction. From our previous discussion, we know that a minority carrier is accelerated by the electrical field inside a reverse biased junction. A majority carrier for the BE junction is a minority one for the CB junction. So, most of the carriers injected in the BE junction will pass to the CB junction. In other words, practically all of the emitter current will pass to the collector.

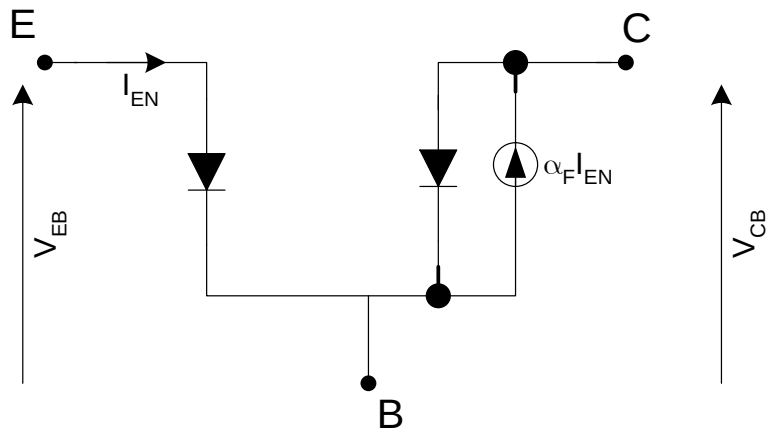


Fig.1-2 PNP transistor in normal operation

We can write $I_C = \alpha_F I_{EN} + I_{C0}$, where α_F is a number that is close to one, I_{EN} is the current in the forward biased BE junction and I_{C0} is the saturation current of the reverse biased CB junction. The collector current will depend only on the injected emitter current and not on the applied voltage between the collector and the base.

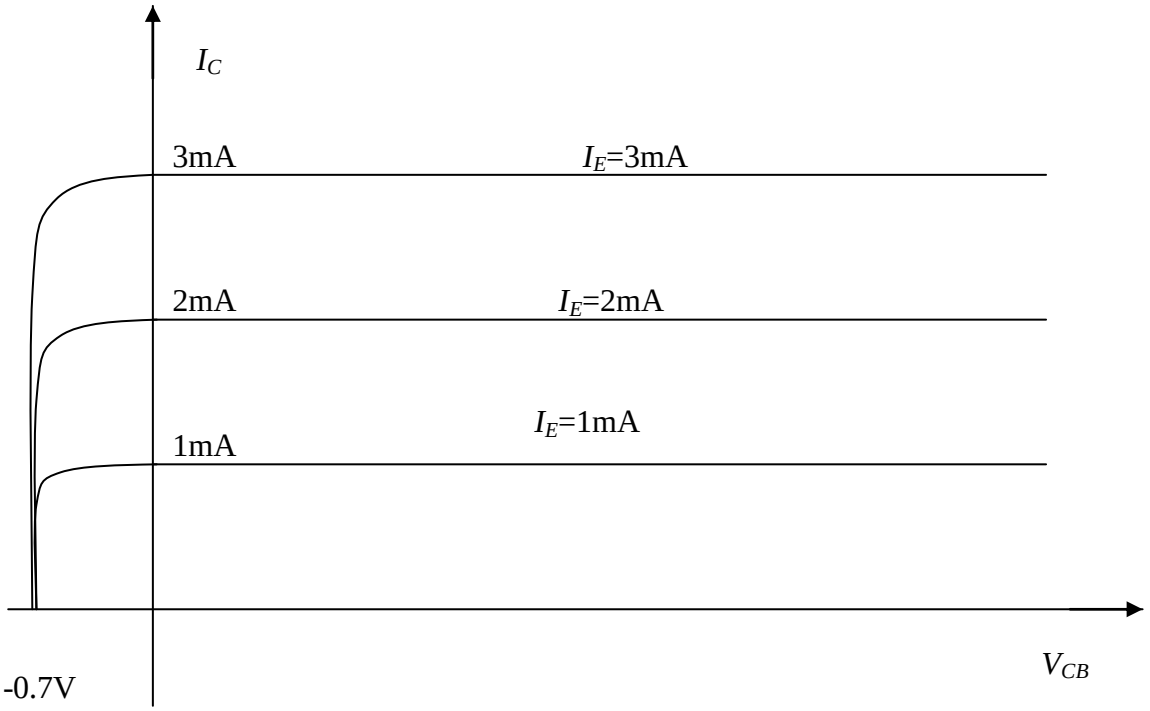


Fig.1-3 Output characteristic for the BJT

The above set of curves shows that the output I-V characteristic of a bipolar junction transistor is just a set of translated diode characteristic.

A more complete model can be obtained if we consider also a reverse transistor (CB forward biased and BE reverse biased). At that time, we can superpose the two transistors and we obtain the "Ebers-Moll" model.

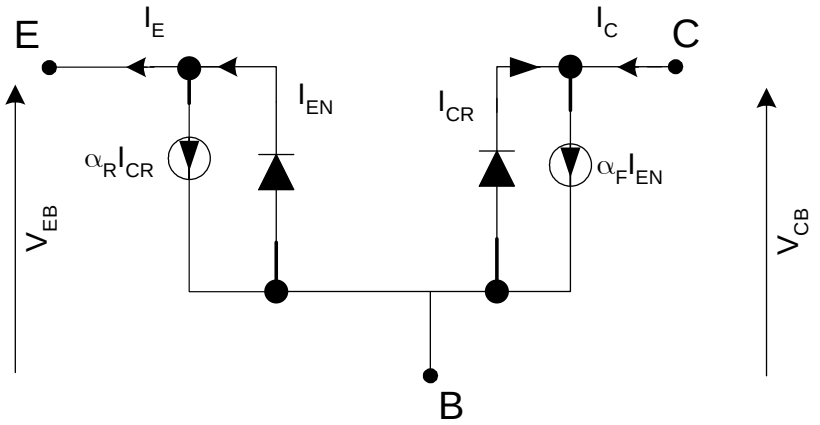


Fig.1-4 The Ebers-Moll model for NPN BJT

The Ebers-Moll model can be summarized by the following set of equations:

$$I_E = I_{EN} - \alpha_R I_{CR}$$
$$I_C = \alpha_F I_{EN} - I_{CR}$$
$$I_E = I_C + I_B$$

And

$$I_{EN} = I_{E0}(e^{\frac{qV_{BE}}{kT}} - 1)$$
$$I_{CR} = I_{C0}(e^{\frac{qV_{BC}}{kT}} - 1)$$

The two saturation currents and the two gains are related via:

$$\alpha_F I_{E0} = \alpha_R I_{C0}$$

The above model is most useful in the analysis of common base circuits. However, most of the circuits will use the BJT in common emitter. If we solve the above equations, we can obtain the following relationship:

$$\frac{I_C}{I_B} = h_{FE} \frac{e^{\frac{qV_{CE}}{kT}} - \alpha_F / \alpha_R}{e^{\frac{qV_{CE}}{kT}} + h_{FE} / h_{FC}}$$

Where:

$$h_{FE} = \frac{\alpha_F}{1-\alpha_F}$$
$$h_{FC} = \frac{\alpha_R}{1-\alpha_R}$$

We see the usual relationship between the collector current and the base current for large V_{CE}, $I_C = \beta I_B$, $\beta = h_{FE}$, but for small values of V_{CE}, we can remark that the output characteristic does not pass by the origin, but all the curves start from a voltage V_{CEsat} given by:

$$V_{CEsat} = \frac{kT}{q} \ln \frac{\alpha_F}{\alpha_R}$$

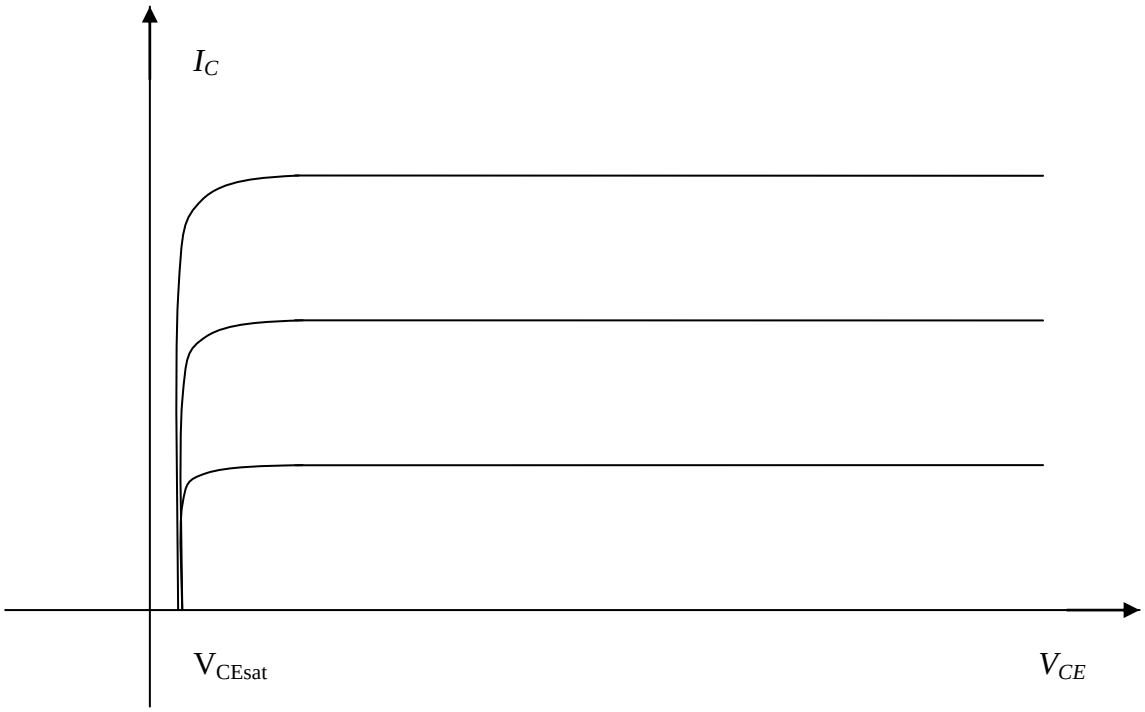


Fig.1-5 I_C-V_{CE} characteristic for several values of I_B

The above relationship does not take into account the "Early effect" which implies a finite output impedance (inversely dependent on the collector current). If we consider the two diodes (BE and CB), we can define four modes of operation of the BJT.

BE forward biased, CB reverse biased: Normal operation.

BE reverse biased, CB forward biased: reverse transistor operation.

BE reverse biased, CB reverse biased: transistor is in cut-off mode.

BE forward biased, CB forward biased: transistor is saturated.

In order to use properly a BJT, we have to bias it correctly, i.e. make sure that under all conditions, the BE junction remains forward biased and the CB junction remains reverse biased. Usually, we select a given "Quiescent" point (Q point), which means a voltage V_{CEQ} and a current I_{CQ} in the above set of curves (Fig. 5) and we use resistors and power supplies in order to achieve the required Q point.

Biasing a BJT

We assume given a Q point V_{CEQ}, I_{CQ}. The simplest biasing network is the following two supply network:

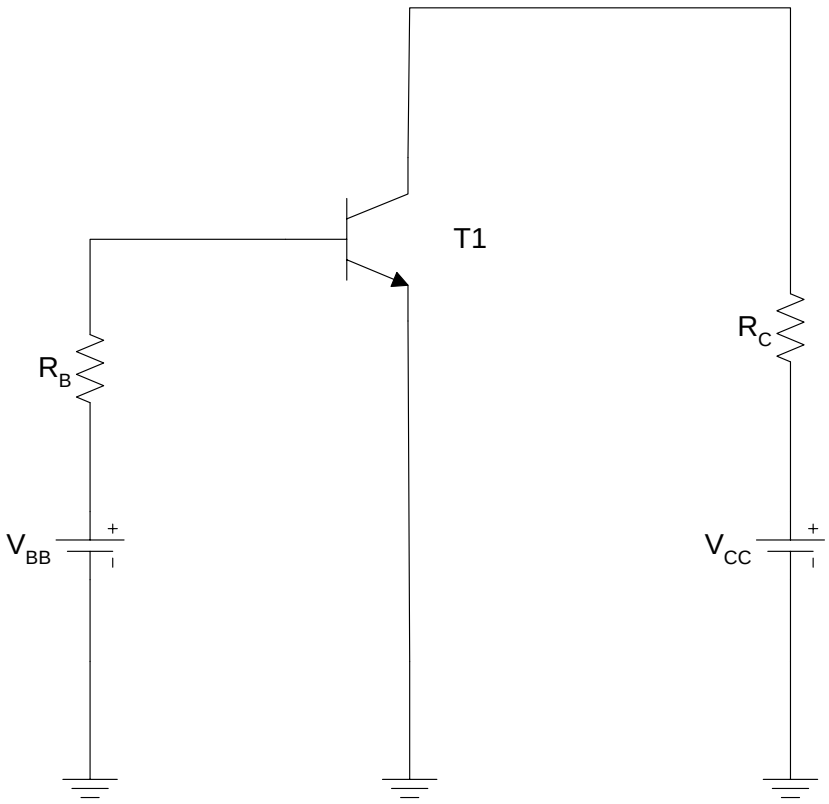


Fig.1-6 Dual supply Biasing

Since we assume that the transistor is correctly biased, the equation governing the BE junction simplifies to :

$$i_E = I_{ES} e^{\frac{qv_{BE}}{kT}}$$

And the Q point is achieved via:

$$V_{BB} = R_B I_{BQ} + V_{BEQ}$$

$$I_{CQ} = \beta I_{BQ}$$

$$I_{EQ} = \frac{I_{CQ}}{\alpha}$$

$$V_{BEQ} = \frac{kT}{q} \ln \frac{I_{EQ}}{I_{ES}}$$

$$V_{CEQ} = V_{CC} - R_C I_{CQ}$$

The above set of equations is a transcendental set and can be solved by successive approximation. However, we make a very small error by assuming that

V_{BEQ} = 650 mV for discrete silicon BJT. Typical values of I_{ES} are about 2 10^{-16} A for integrated silicon transistor, 2 10^{-14} A for a discrete silicon transistor and about 2 10^{-7} A for a germanium transistor. Solving for V_{BEQ} for emitter currents between 0.1 mA and 10 mA produce a BE voltage that remains around 650 mV for a discrete Si transistor, 750 mV for an integrated one and 220 mV for a Ge transistor.

Since the two batteries have the same polarity, we can simplify the circuit and use a single power supply. At that time the circuit becomes:

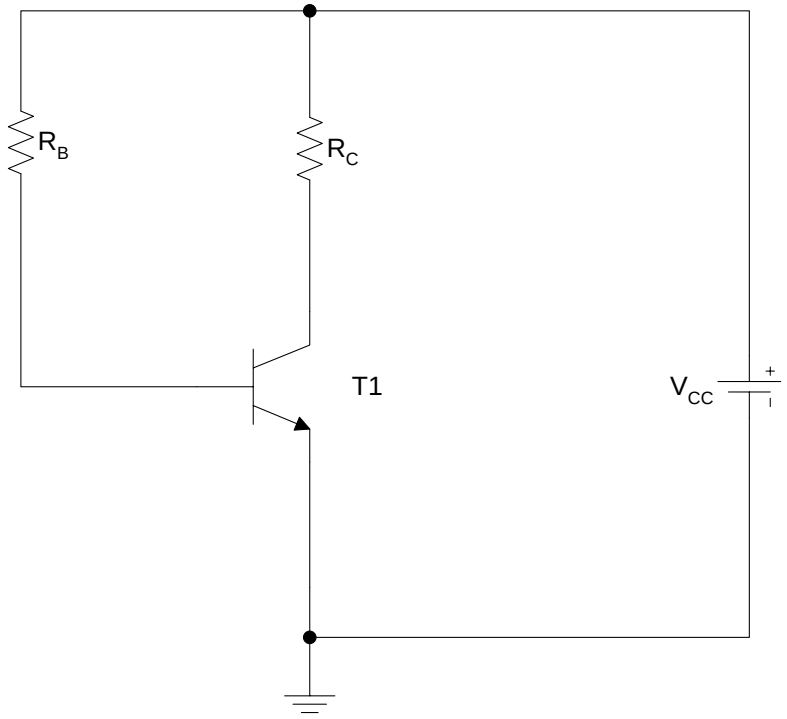


Fig.1-7 Single battery biasing

We can apply the same set of equations as for the previous circuit by replacing V_{BB} by V_{CC}.

Example 1:

Consider the circuit of Fig.7 with a transistor having I_{ES}=2 10^{-14} A, R_B = 1 MΩ, R_C = 5 kΩ, β = 120, V_{CC} = 10V. Compute I_{CQ} and V_{CEQ}.

With β = 120, we obtain α = 0.9917. We have to compute I_{CQ}. We start the iteration by assuming a value of V_{BEQ} = 650 mV. This provides the following values for the different currents:

I_{BQ}= 9.35 μA, I_{CQ}=1.1 mA and I_{EQ}=1.1 mA, replacing in $V_{BEQ} = \frac{kT}{q} \ln \frac{I_{EQ}}{I_{ES}}$, we obtain V_{BEQ} = 643.7 mV. Another iteration will produce the same values. So, we can say that I_{CQ} = 1.1 mA and this provides $V_{CEQ} = V_{CC} - R_C I_{CQ}$ = 4.39 V.

Example 2:

Consider the same circuit with a transistor having $50 \le \beta \le 300$. We want to bias it around the Q point I_{CQ} = 1 mA and V_{CEQ} = 5 V. Because of the wide spread of the different values of β, we are going to use the geometric mean of 300 and 50. So $\beta = \sqrt{50 \times 300}$ = 122. This provides I_{BQ} = 8.2 μA and R_B = 1.14 MΩ. R_C = 5 kΩ.

If we use these resistors with a transistor having an actual β = 50, the collector current will reduce to: I_{CQ} = 0.4 mA. And this will imply a collector voltage V_{CEQ} = 8 V. So, if the output ac voltage exceeds 2 V peak, we will have distortion by cut-off.

If the true β = 300, then $I_{CQ} = \beta I_{BQ}$ = 2.4 mA and this collector current will produce a drop of voltage of 12 V across R_C, which is evidently impossible. This simply means that the transistor will be saturated at its Q point and $V_{CEQ} = V_{CEsat}$ while I_{CQ} will be given by $I_{CQ} = \frac{V_{CC} - V_{CEsat}}{R_C}$.

Example 2 shows clearly that the above method of biasing is too dependent on the value of β, and for most transistors, the fabricant can only guarantee that β is within a wide spread of values. So, instead of trying to impose the base current, a better method will consist of imposing the emitter current, since the relation between emitter and collector current is via α which is always very close to one.

The next circuit that we will study will impose the emitter current via a negative power supply.

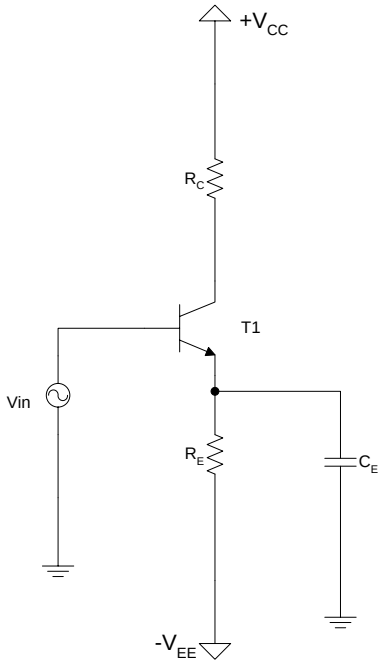


Fig.1-8 biasing using a negative supply

For the above circuit, the ac source is directly coupled to the base. From the dc point of view, the base is directly connected to ground. So, the capacitor C_E will charge to $V_{DCQ} = V_{EBQ}$ (we assume that $V_{in} = 0$ V, if $V_{in} \neq 0$, then due to the non linearity of the base-emitter junction, the voltage across the capacitor will depend on the ac voltage also). We can compute the quiescent emitter current:

$$I_{EQ} = \frac{V_{EE} - V_{DCQ}}{R_E}$$

$$I_{CQ} = \alpha I_{EQ}$$

$$V_{CEQ} = V_{CC} - R_C I_{CQ}$$

It is evident that changing the transistor will not affect (significantly) the Q point and if $V_{EE} >> V_{DCQ}$, then the emitter current can be set with a very high precision. The capacitor C_E is a by-pass capacitor. Its impedance should be smaller than the impedance in parallel at the lowest frequency. The impedance in parallel with C_E is the parallel combination of R_E and the dynamic resistance $r_e = \left.\frac{dv_{BE}}{di_E}\right|_{i_E = I_{EQ}} = \frac{kT}{qI_{EQ}}$ which is usually much smaller.

If we cannot use a negative power supply, we can use the same circuit if we raise the dc voltage level of base. We can use a voltage divider to do so.

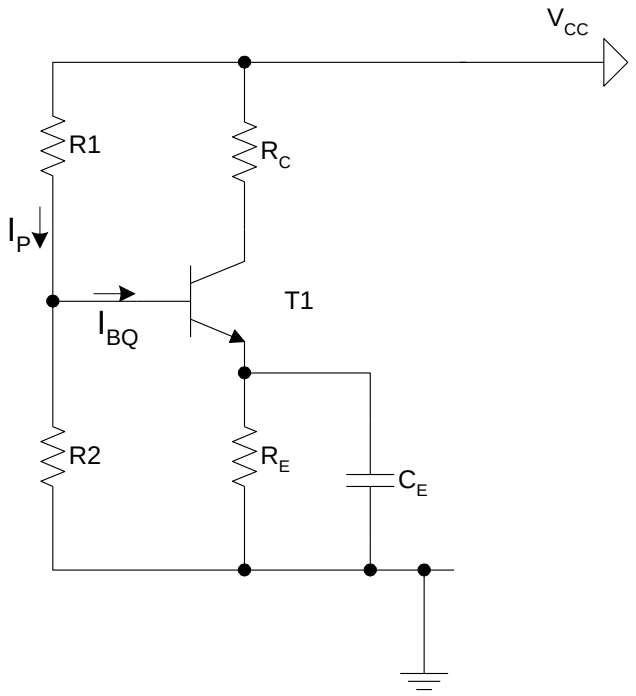


Fig.1-9 single supply resistive biasing

The Thevenin equivalent circuit of the base emitter circuit is

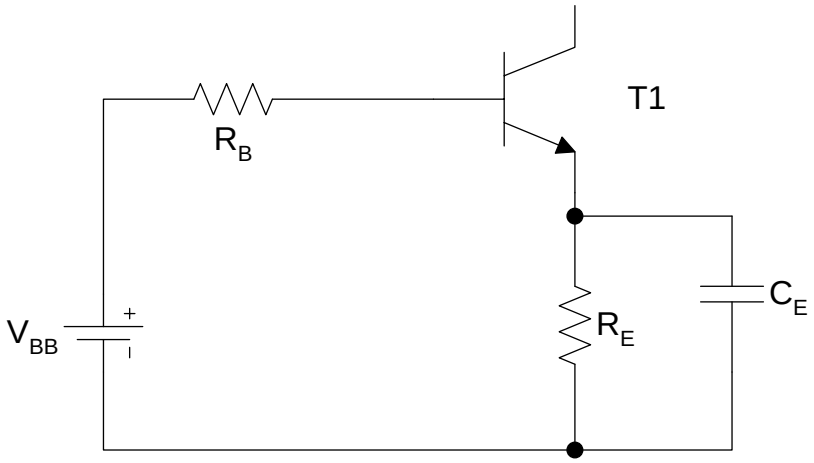


Fig.1-10 Base emitter equivalent circuit

Where:

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Using the circuit of Fig.1-10, we obtain the following equations:

$$V_{BB} = R_B I_{BQ} + V_{BEQ} + R_E I_{EQ}$$
$$I_{BQ} = (1-\alpha) I_{EQ}$$

This provides:

$$I_{EQ} = \frac{V_{BB} - V_{BEQ}}{R_E + (1-\alpha) R_B}$$
$$V_{BEQ} = \frac{kT}{q} \ln \frac{I_{EQ}}{I_{ES}}$$

And:

$$V_{CEQ} = V_{CC} - R_C I_{CQ} - R_E I_{EQ}$$
$$I_{CQ} = \alpha I_{EQ}$$

We will come back to the previous circuit later in the course. We are going to see methods for biasing the circuit of Fig.1-9. The first method is based of the stability factor $S_{V_{BE}} = \frac{\partial I_{CQ}}{\partial V_{BE}}$. Using the above equations, we obtain:

$$S_{V_{BE}} = \frac{-\alpha}{R_E + (1-\alpha) R_B} \approx \frac{-1}{R_E}$$

We know that the base emitter voltage has a variation that is inversely proportional to variation of the temperature, $\Delta V_{BEQ} = -2.2mV\ /°\text{C} \times \Delta T$, so, if we are given a variation of I_{CQ} for a given variation of temperature ΔT , we can compute the value of R_E and then R_B such that $(1-\alpha) R_B \leq R_E / 10$.

Example 3:

We want to bias a 2N3904 transistor having $\beta_{\min} = 50$ with ICQ = 1 mA and we can tolerate a variation of $\pm 10\%$ of collector current when the ambient temperature varies by $\pm 30°\text{C}$, the power supply is 10 V.

$\Delta T = 30°\text{C}$, so $\Delta V_{BE} = -2.2mV\ /°\text{C} \times 30°\text{C} = -66mV$, so

$$R_E = -\frac{\Delta V_{BE}}{\Delta I_{CQ}} = \frac{66mV}{0.1mA} = 660\,\Omega$$

And then, since $(1-\alpha) = \frac{1}{\beta+1}$, we obtain

$$R_B = \frac{(\beta+1) R_E}{10} = \frac{51 \times 660}{10} = 3366\,\Omega$$

We leave the remaining calculation as homework (Compute R1, R2, R_C and C_E).

You should note that we have used the value of $\beta_{\min}$. It is because it corresponds to the maximum value of I_{BQ}.

Another method of design is to use the following rule of thumb.

The voltage V_E across the capacitor C_E should be set to a value of about 10% of V_{CC} as long as it is larger than 1 V. A smaller value of V_E will lead to thermal instability. The voltage divider current I_P should be set to a value that is at least equal to ten times the maximum base quiescent current. We can repeat the same design as in example 3.

$$V_E = \frac{V_{CC}}{10} = 1V \text{ so } R_E = \frac{1V}{1\,mA} = 1\,k\Omega,\ I_{BQ\max} = \frac{I_{CQ}}{\beta_{\min}} = \frac{1\,mA}{50} = 20\,\mu A$$

The current I_P is given by: $I_P = I_{BQ\max} \times 10 = 0.2\,mA$ so the sum of the two resistors *R1* and *R2* is given by: $R1 + R2 = \frac{V_{CC}}{I_P} = \frac{10V}{0.2\,mA} = 50\,k\Omega$ and the voltage at the base of the transistor is:

$$V_B = V_{CC}\frac{R2}{R1+R2} = V_E + V_{BEQ} = 1V + 0.65V = 1.65V \text{ and we obtain}$$

R2 = 8.25 kΩ and *R1* = 41.75 kΩ. The bypass capacitor can be computed if we know the lowest frequency to be amplified. Let us assume that it is 100 Hz.

The dynamic resistance of the base emitter junction is:

$$r_e = \frac{kT}{qI_{EQ}} = \frac{26\,mV}{1\,mA} = 26\,\Omega$$

So if $|Z_{CE}| = \frac{1}{2\pi f C_E} \simeq \frac{r_e}{10}$, we obtain $C_E = 612\,\mu F$.

The next biasing system consists of replacing the emitter resistor R_E by a current source. The type of current source we will demonstrate is the current mirror which commonly used in integrated circuits. This circuit is shown in Fig.1-11.

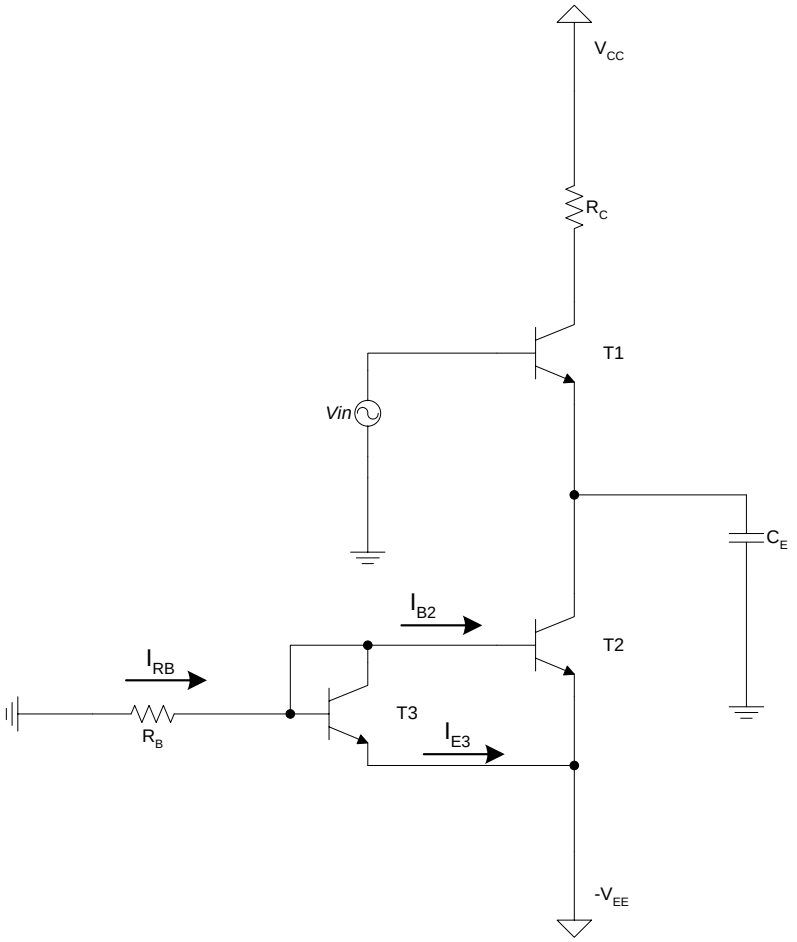


Fig.1-11 Biasing using a current mirror

Since we are considering integrated circuits, we can always take for granted that the only way that two transistors will differ will be through their geometry. So, if we use the same masks to diffuse the two transistors, they will be identical. So, in the analysis of the above circuit, we assume that T2 and T3 are identical, which means that $I_{ES_2} = I_{ES_3}$. For each transistor, we can write $I_{Ek} = I_{ES_k} e^{\frac{qV_{BE_k}}{kT}}$, and if we consider T2 and T3, we can remark that $V_{BE_2} = V_{BE_3}$ so $I_{E_2} = I_{E_3}$. The transistor T2 is connected as a diode with the collector and the base shorted. It is quite common to use transistors as diodes in integrated circuits. They occupy the same silicon area and it is easier to achieve identical transistors than identity between a diode and a transistor. The currents obey: $I_{RB} = I_{B2} + I_{E3}$. Since the transistors are identical, they have the same α. So, we can write: $I_{RB} = (2 - \alpha)I_{E2}$. We finally obtain the following equation for the current I_{E2}:

$$I_{E2} = \frac{V_{EE} - V_{BE2}}{(2-\alpha)R_B}$$

And of course: $I_{C2} = \alpha I_{E2}$ and we can use the value of 750 mV for V_{BE2}. We can remark that if $\alpha = 1$ then $I_{C2}=I_{RB}$, so the circuit mirrors the current I_{RB} which is produced by a non ideal current source to the current I_{C2} which is the collector current of T2 and as long as V_{CE2} is larger than V_{CEsat}, the transistor T2 will behave as an ideal current source. So, as long as the lower pair of transistors behaves as a current source, we can replace it in the schematic and we obtain the following schematics.

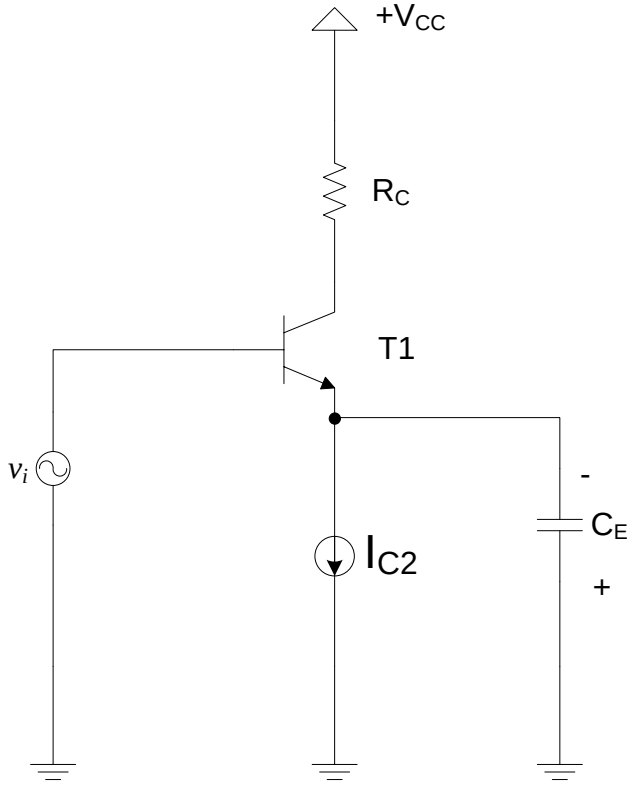


Fig.1-12 Biasing using a current source

The model of Fig.1-12 is the simplest one to analyze because the dc current is fixed by the current source and it does not depend on a voltage drop across a resistor.

It is interesting to compute the dc voltage stored in the capacitor C_E. We are going to show that it depends on the applied voltage v_i. The base emitter voltage v_{BE} is the sum of the ac voltage v_i and the capacitor voltage V_{DC} .

$$v_{BE} = v_i + V_{DC}$$

When $v_i = 0$, the capacitor is charged to:

$$V_{DCQ} = \frac{kT}{q} \ln \frac{I_{C2}}{I_{ES}}$$

When $v_i \neq 0$, the capacitor charges to a different value V_{DC}. This is due to the non linearity of the transistor that does not amplify in the same way the two alternances of the ac signal. Since the circuit is non linear, we cannot analyze it for a general signal, so we assume that the input ac signal is sinusoidal: $v_i = V_1 \cos \omega_0 t$

$$i_E = I_{ES} e^{\frac{qv_{BE}}{kT}} = I_{ES} e^{\frac{qV_{DC}}{kT}} e^{\frac{qV_1}{kT}\cos \omega_0 t}$$

$$= I_{ES} e^{\frac{qV_{DC}}{kT}} e^{x \cos \omega_0 t}$$

Where $x = \frac{qV_1}{kT}$.

We can remark that the output current is not sinusoidal.

$$i_C(t) = \alpha i_E(t)$$

$$v_C(t) = V_{CC} - R_C i_C(t)$$

The current i_E is periodic and it can be developed in Fourier series.

$$e^{x \cos \omega_0 t} = I_0(x) + 2\sum_{n=1}^{\infty} I_n(x) \cos n\omega_0 t$$

$I_n(x)$ is the modified Bessel function of the first kind, of order n and argument *x*.

We obtain finally:

$$i_E = I_{ES} e^{\frac{qV_{DC}}{kT}} I_0(x) \left[1 + \sum_{n=1}^{\infty} \frac{2I_n(x)}{I_0(x)} \cos n\omega_0 t \right]$$

Thus, the average value of the emitter current $< i_E >$ is:

$$< i_E > = I_{ES} e^{\frac{qV_{DC}}{kT}} I_0(x)$$

And it must be equal to I_{C2}, since it is the only dc current present in the circuit and no dc current can flow in a capacitor. The fundamental and the harmonics of i_E will flow through the by-pass capacitor, so we have the following expression for the emitter current:

$$i_E = I_{C2} \left[1 + \sum \frac{2I_n(x)}{I_0(x)} \cos n\omega_0 t \right]$$

And we can compute the capacitor voltage from the expression of <i_E>:

$$V_{DC} = \frac{kT}{q}\ln\frac{I_{C2}}{I_{ES}I_0(x)} = \frac{kT}{q}\ln\frac{I_{C2}}{I_{ES}} - \frac{kT}{q}\ln I_0(x)$$

$$= V_{DCQ} - \frac{kT}{q}\ln I_0(x)$$

We remark that this voltage depends on *x*, i.e. on V_1.

1.4 The Field Effect Transistor.

The field effect transistor operation is not based on the transformation of majority carriers into minority ones but on the modification of the conduction of a channel by an electrical field. The field can be developed inside a depletion region of a reverse biased PN junction (junction FET or JFET) or using the electrical field developed inside a capacitor (metal oxide semi-conductor or insulated gate FET, MOSFET, IGFET). In MOSFET, the channel can be depleted as in JFET or it can be enhanced. The following figures show a simplified structure of the different FET transistors along with the associated symbol.

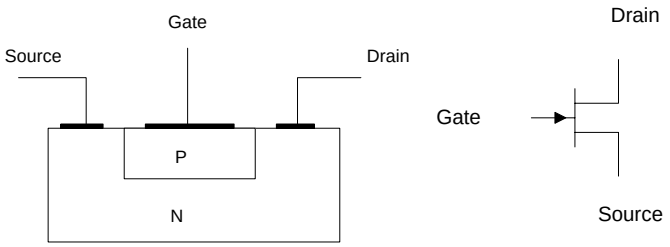


Fig.1-13 N-channel JFET structure and symbol.

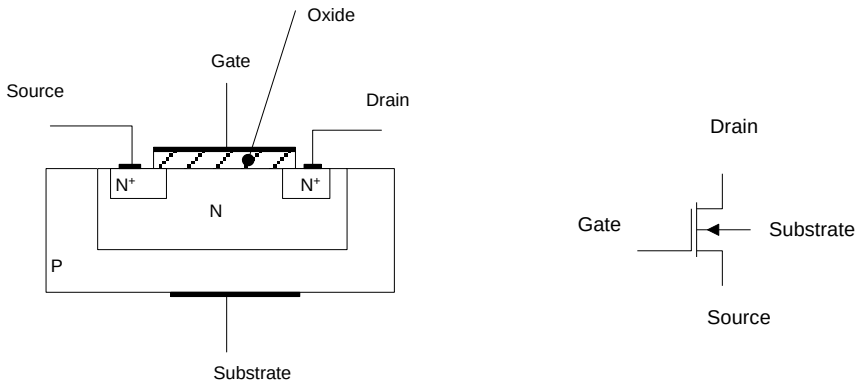


Fig.1-14 Depletion mode N-channel MOSFET structure and symbol

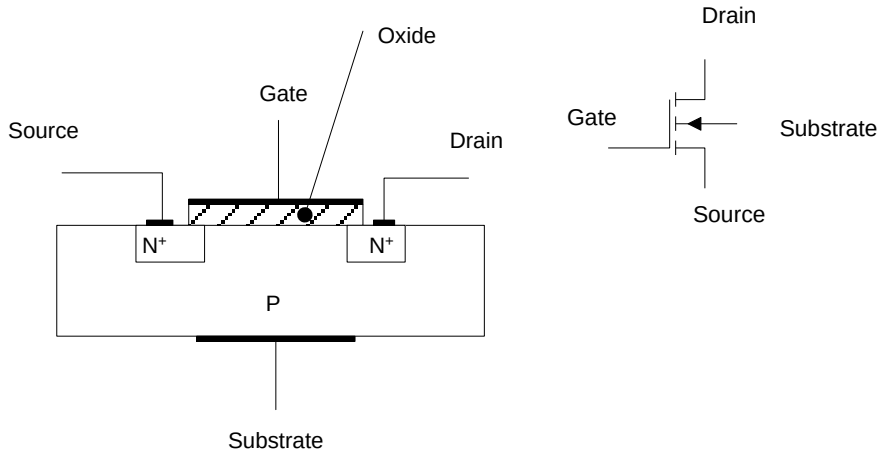


Fig.1-15 Enhancement mode N-channel MOSFET and symbol

The arrow in the different symbols indicates the conducting direction of the PN junction (gate-channel or substrate channel). If the channel is of P type, then the arrow should be reversed.

The different FET transistors have a half square law transfer characteristic (I_D, V_{GS}). We start with the description of the N channel JFET transistor. It is evident that the gate-channel diode should never be forward biased. So, in normal use, the gate voltage should always be lower than the source voltage. A good approximation for the transfer characteristic is:

$$i_D = I_{DSS}\left(1-\frac{v_{GS}}{V_P}\right)^2 \qquad V_P \le v_{GS} \le 0$$

$$= 0 \qquad v_{GS} < V_P$$

The above relation is valid for a drain source voltage $v_{DS} \ge |V_P|$. This transfer characteristic is plotted below (Fig.1-16). I_{DSS} is the drain saturation current and $|V_P|$ is the pinch off voltage.

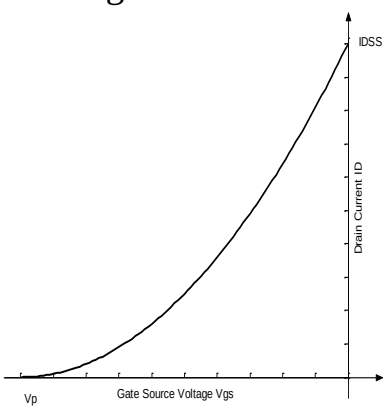


Fig.1-16 N channel JFET transfer characteristic

The output curves (I_D, V_{DS}) of the FET transistor are also quite different from the ones of the BJT. The following curves are ideal in the sense that the output impedance of the FET transistor is assumed to be infinite.

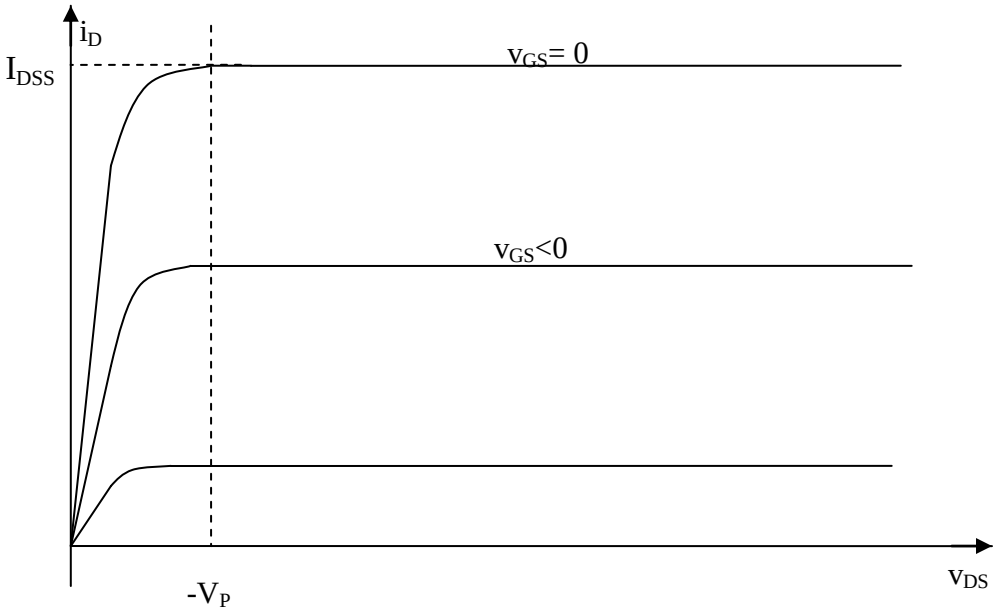


Fig.1-17 Output curves i_D vs v_{DS}

We can remark two distinct regions in the above curves. In the area corresponding to $v_{DS} > -V_P$, the transistor behaves as a current source (controlled by v_{GS}). It is called the saturation region and it corresponds to the complete pinch off of the channel. It is the normal operating region. The other region is called the ohmic region. For small values of v_{DS}, the resistance of the drain to source channel is variable and is controlled by the gate to source voltage v_{GS}.

For v_{DS} limited to a few hundreds of millivolts, we can use the following expression:

$$R_{DS} = \frac{V_P^2}{2I_{DSS}(v_{GS} - V_P)} \qquad V_P \le v_{GS} \le 0$$

and we can use the JFET as a variable resistor in circuits. The above relation is valid even if v_{DS} is negative as long as it is small enough.

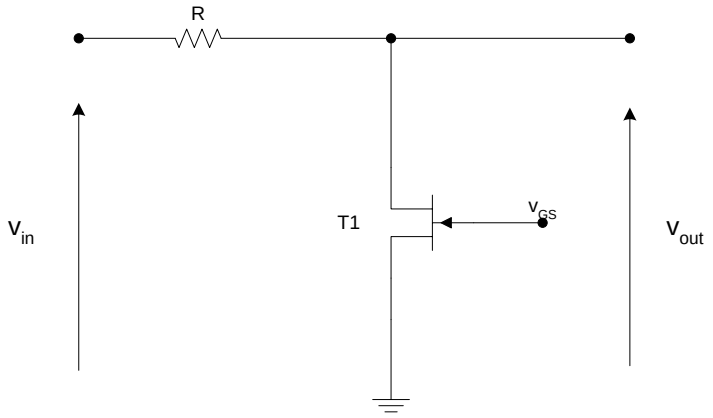


Fig.1-18 Voltage controlled attenuator

The above circuit is an example of a voltage controlled attenuator. If we assume zero source impedance and infinite load impedance, its transfer is given by:

$$\frac{v_{out}}{v_{in}} = \frac{R_{DS}}{R + R_{DS}}$$

as long as $|v_{out}|$ is limited to few hundreds of millivolts. The smallest value of R_{DS} is usually called R_{on} when we use the FET as a switch. If the control voltage v_{GS} is a square wave varying between 0V and $V_{min} < V_P$ and if $R >> R_{on}$, then the above circuit can be used as a chopper (for modulators).

Biasing the JFET

Biasing the JFET means fixing the values of I_{DQ} and V_{DSQ}. The following circuit provides a very simple way of achieving the above Q point.

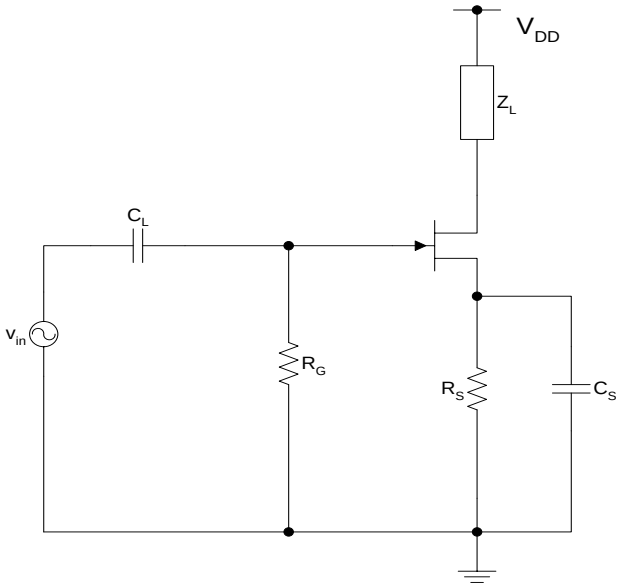


Fig.1-19 Biasing using a source resistor.

The above biasing circuit is based on the fact that the gate to source diode is reverse biased (under normal operation) and that there is practically no current that flows through the resistor R_G. So, the biasing relations are:

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2$$

$$-V_{GSQ} = R_S I_{DQ}$$

And $V_{DSQ} = V_{CC} + V_{GSQ}$ if the capacitor C_S is large enough so that its voltage remains constant when i_D varies and if there is no dc drop across the load Z_L. We can guarantee the above result if the impedance of the capacitor is much smaller than the impedance connected in parallel which is R_S in parallel with the inverse of the small signal transconductance at the Q point $(1/g_{mQ})$ at the lowest operating frequency. A graphical representation of the above relations is shown below:

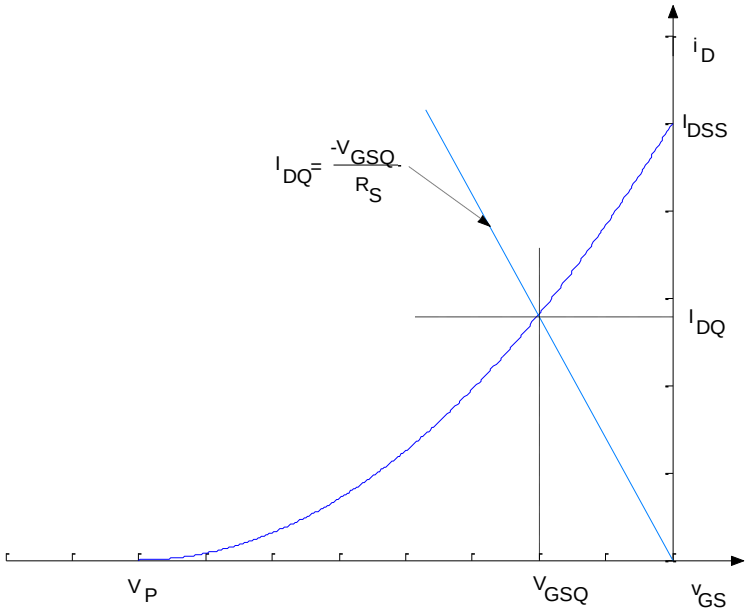


Fig.1-20 Biasing using a source resistor

The R_G resistor should be such that the gate voltage is as close to zero volts as possible. You can find the maximum reverse gate source current in manufacturers' data sheets. The main problem with the above circuit is the fact that the Q point is highly dependent on the transistor parameters I_{DSS} and V_P. A smaller variation of I_{DQ} is provided by the following circuit (based on a higher voltage across the resistor R_S.

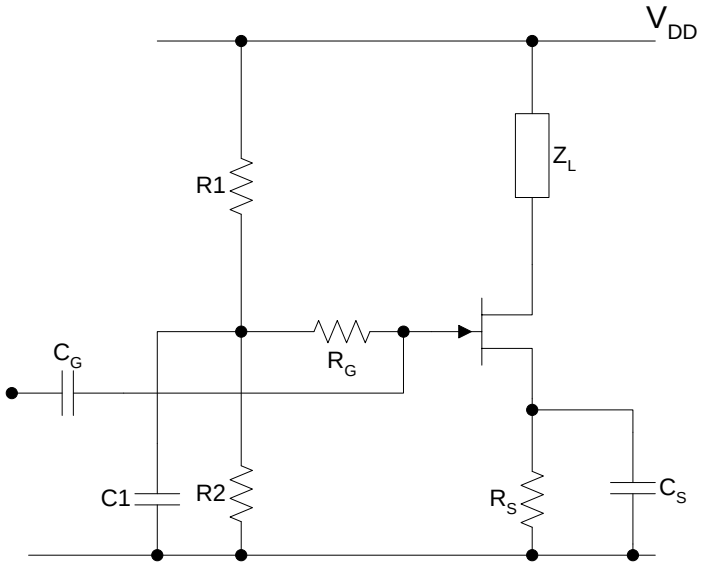


Fig.1-21 Biasing a JFET using a source resistor and a gate voltage.

The voltage divider R1, R2 raises the gate voltage to $V_{GG}=V_{DD}\frac{R2}{R1+R2}$. At that time, the biasing load line becomes $V_{GG}-V_{GSQ}=R_S I_{DQ}$ which is represented in the figure below. We can remark the small variation of I_{DQ} when we change the transistor.

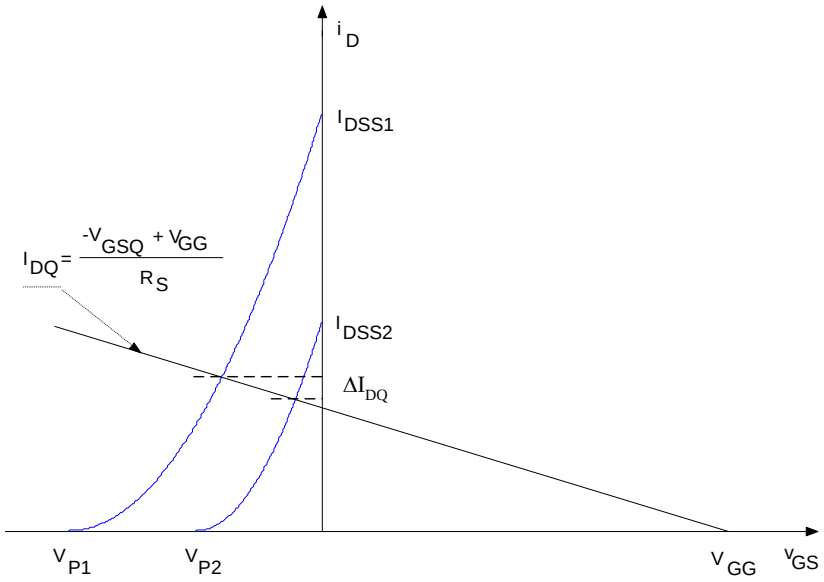


Fig.1-22 biasing a JFET using a source resistor and a gate voltage

The different MOS transistors obey a transfer characteristic which also square law. However, the gate source voltage is not restricted to negative voltages. The transfer characteristic of a MOSFET is thus:

$$i_D = \beta(v_{GS} - V_{th})^2 \qquad v_{GS} \geq V_{th}$$
$$i_D = 0 \qquad v_{GS} < V_{th}$$

If the transistor is of depletion mode, the threshold voltage V_{th} is negative and for enhancement mode MOSFET, it is positive.

The biasing circuits for depletion mode MOSFET can be the same as the ones described above for JFET. The value of the gate resistor can be much higher since the input of the transistor is a capacitor and not a reverse biased diode. The depletion mode MOSFET can even be biased with $V_{GSQ} = 0V$ because v_{GS} can be positive.

The biasing circuits of enhancement mode MOSFET will be the same as the one shown in Fig.1-21. The biasing load line is the same as the one shown in Fig.1-22, with the transfer characteristic translated to the right.

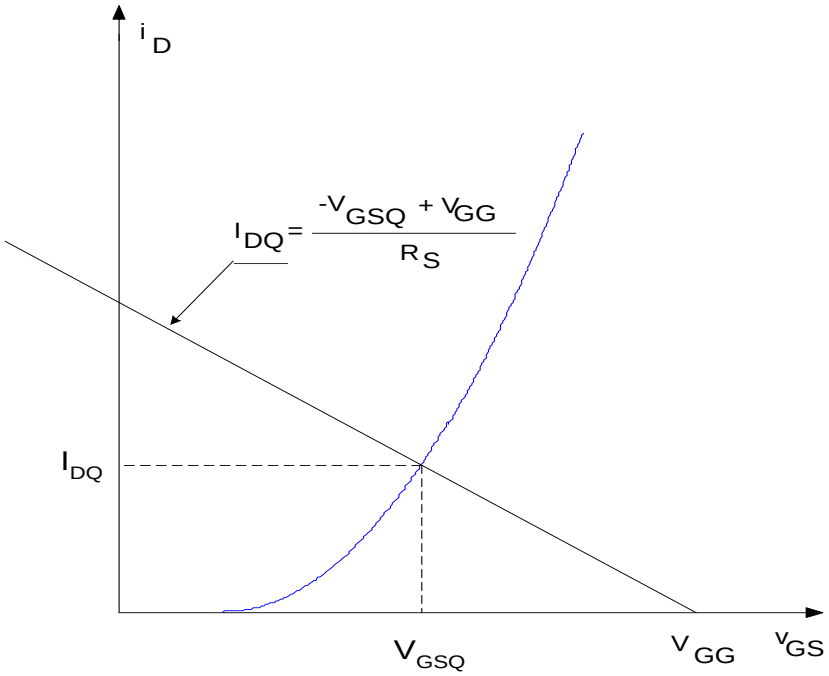


Fig.1-23 biasing an enhancement mode MOSFET

If we want to avoid any variation of the biasing current I_{DQ}, we can use a current source to provide the current.

Chapter 2

Passive frequency dependent networks

and transformer like networks

Practically all CW communication circuits are band pass circuits. A typical circuit consists of a cascade of active devices and passive networks. The passive networks are used to couple circuits together, to select a particular band of frequency around some carrier and to match impedances. The basic building elements of these networks are: resistors, capacitors, inductors and transformers (mutual inductance).

2.1 Impedance and Admittance

One port networks are characterized by a relationship between the voltage across the device and the current through the device. If the device is composed of resistors, capacitors or inductors, the relationship is linear and time invariant.

The resistor is characterized by a memoryless relationship:

$v(t) = Ri(t)$ between time domain variables, $V = RI$ between phasors and the same relation between Laplace transformed variables $V(s) = RI(s)$.

The capacitor and the inductor have a differential relationship:

$v(t) = L\frac{di(t)}{dt}$ and $v(t) = \frac{1}{C}\int_{-\infty}^{t} i(\lambda)d\lambda$ in the time domain, $V = jL\omega I$ and $V = \frac{1}{jC\omega}I$ between phasors and $V(s) = LsI(s)$ and $V(s) = \frac{1}{Cs}I(s)$ between Laplace transformed variables. Each one of the devices is characterized by an attribute: Resistance for the resistor, inductance for the inductor and capacitance for the capacitor. When we consider relations between phasors, the current and the voltage across the one port device is a complex number. It is a function of either the complex number $s = \sigma + j\omega$ or just the purely imaginary number $j\omega$.

The impedance is the complex number:

$Z(j\omega) = R(j\omega) + jX(j\omega)$, the real part $R(j\omega)$ is called the resistance of the circuit and the imaginary part $X(j\omega)$ is the reactance of the circuit. The current and the voltage for a general one port network are related by:

$$V(j\omega) = Z(j\omega)I(j\omega)$$

The inverse relationship $I(j\omega) = Y(j\omega)V(j\omega)$ is provided by the admittance:

$Y(j\omega) = G(j\omega) + jB(j\omega)$. The real part $G(j\omega)$ is called the conductance of the circuit and the imaginary part is called the susceptance of the circuit.

If the network is passive, the resistance (the conductance) of the network is always positive. The one port network will be inductive if $X(j\omega) > 0$ ($B(j\omega) < 0$). The network will be capacitive if $X(j\omega) < 0$ ($B(j\omega) > 0$).

Parallel series transformations

One port networks can be seen either as a series representation of a resistance and a reactance or as a parallel combination of a conductance and a susceptance.

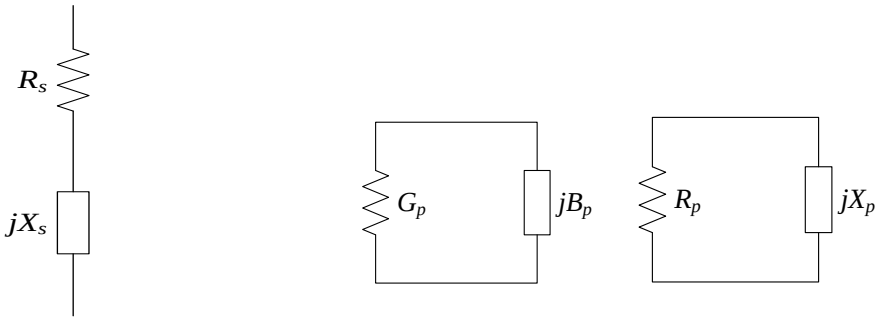


Fig.2- 1 Series parallel transformations

As shown in the above figure, we have three possible representations of the same impedance. We can thus write the following relations:

$$Z = R_s + jX_s$$

$$Y = G_p + jB_p = \frac{1}{R_p} + \frac{1}{jX_p}$$

Since $Y = \frac{1}{Z}$, we have the following equations:

$G_p = \frac{R_s}{R_s^2 + X_s^2}$ and $B_p = \frac{-X_s}{R_s^2 + X_s^2}$. These relations are often stated as a function of the quality factor of the impedance. The quality factor Q is defined as:

$$Q = \left|\frac{X_s}{R_s}\right| = \left|\frac{B_p}{G_p}\right| = \left|\frac{R_p}{X_p}\right|$$

The "Que" of the circuit indicates how reactive the circuit is. A pure reactance will have Q = ∞.

$$G_p = \frac{1}{R_s\left(1+Q^2\right)};\ \ B_p = \frac{-Q^2}{X_s\left(1+Q^2\right)}.$$

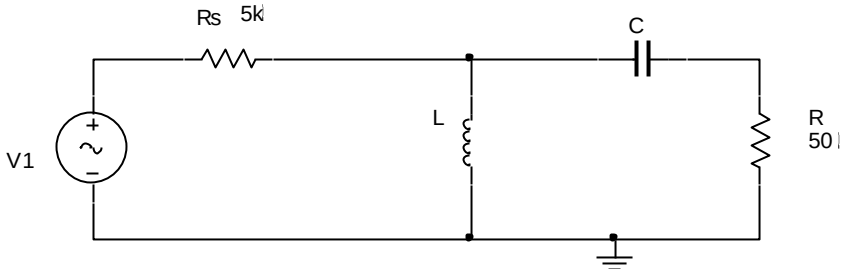
The above expressions are frequently given in terms of R_p and X_p:

$R_p = R_s\left(1+Q^2\right)$ and $X_p = \dfrac{X_s\left(1+Q^2\right)}{Q^2}$. If Q ≥10, these relations simplify to: $R_p \simeq R_s Q^2$ and $X_p \simeq X_s$ (with an error of less than 1%).

We can use the above relations to solve single frequency matching problems as shown in the following example.

Example:

We want to match a 50 Ω load to a source having a resistance of 5 kΩ at the frequency of 1 MHz. We can use the following network:



If we use the above approximate formula, we can transform the series combination of *C* and *R* to parallel C_p and R_p.

$R_p = Q^2 R$ giving Q^2 = 100 or Q = 10. This value of Q justifies the use of the approximate relation. From $Q = \left|\dfrac{B_p}{G_p}\right|$, we obtain: $|B_p| = C\omega = QG_p$ ($C_p = C$). This provides:

C = 318 pF, we use the standard value *C* = 330 pF. *L* is used to cancel the reactance of *C*: $L\omega = \dfrac{1}{C\omega}$ giving *L* = 79 μH. We can use this value if we build the inductor or use the standard value *L* = 82 μH.

2.2 Two port networks

In this chapter, we are going to study coupling networks. These networks are used to filter signals and match impedances.

Linear time invariant two port networks are characterized by matrices relating the different variables. The variables represent small ac voltages and currents.

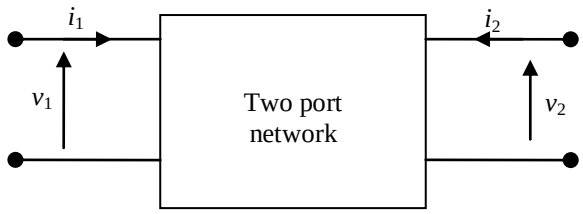


Fig.2- 2 Two port network

Any pair of variables from (i_1, i_2, v_1, v_2) can be associated with the other pair of variables. Two of the commonly used parameters are: the "z" (open circuit) or impedance parameters and the "y" (short circuit) or admittance parameters.

The impedance parameters are described by the following set of equations:

$$v_1 = z_{11} i_1 + z_{12} i_2$$

$$v_2 = z_{21} i_1 + z_{22} i_2$$

or in matrix form:

$$\begin{pmatrix} v_1 \\ v_2 \end{pmatrix} = \begin{pmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \end{pmatrix}$$

$z_{11} = \left.\frac{v_1}{i_1}\right|_{i_2=0}$ is the input impedance for an open output port.

$z_{12} = \left.\frac{v_1}{i_2}\right|_{i_1=0}$ is the reverse transimpedance for an open input port.

$z_{21} = \left.\frac{v_2}{i_1}\right|_{i_2=0}$ is the forward transimpedance for an open output port.

$z_{22} = \left.\frac{v_2}{i_2}\right|_{i_1=0}$ is the output impedance for an open input port.

The two port network is said to be reciprocal when the open circuit voltage measured at one port due to a current excitation at the other port is unchanged when the measurement and excitation ports are interchanged.

In this case, $z_{12} = z_{21}$. The proof is left as an exercise. A network containing only R, L, C and M elements is always reciprocal.

The two port is said to be unilateral if the reverse transimpedance is zero: $z_{12} = 0$. In this case, there is no feedback from the output port to the input one.

The disadvantage of the impedance parameters is the fact that they are difficult to measure. One port must be open during the measurement. The parasitic capacitances will affect the measurement. This problem does not exist with the admittance parameters since they are short circuit parameters.

The admittance parameters are described by the following set of equations:

$$i_1 = y_{11}v_1 + y_{12}v_2$$
$$i_2 = z_{21}v_1 + z_{22}v_2$$

or in matrix form:

$$\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} = \begin{pmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix}$$

$y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0}$ is the input admittance for an shorted output port.

$y_{12} = \left.\frac{i_1}{v_2}\right|_{v_1=0}$ is the reverse transadmittance for an shorted input port.

$y_{21} = \left.\frac{i_2}{v_1}\right|_{v_2=0}$ is the forward transadmittance for an shorted output port.

$y_{22} = \left.\frac{i_2}{v_2}\right|_{v_1=0}$ is the output admittance for an shorted input port.

It is evident that the (Z) matrix is the inverse of the (Y) matrix and vice versa. Since the elements of the (Y) matrix are easier to measure at medium and high frequency, the "y" parameters are commonly used to design HF, VHF and even UHF amplifiers. At higher frequencies, it is better to use distributed parameters such as the scattering parameters.

2.3 Mutual Inductance and transformer

A commonly used two port network consists of two inductors coupled magnetically: the transformer.

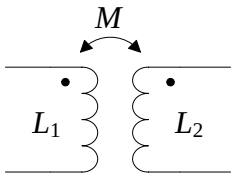


Fig.2- 3 Mutual Inductance

The winding corresponding to L_1 is called the primary, the other is the secondary. The dots indicate the way the transformer is wound. The coupling is due to the mutual inductance *M*. With the dots positioned as in Fig.2- 3, the

mutual inductance is positive. If the two coils are wound in opposing direction, the value of *M* will be negative and the dots will be drawn on opposing ends of the windings.

The basic equations are:

$$v_1(t) = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}$$

$$v_2(t) = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt}$$

If we consider the transfer of energy in the transformer, we can show that $M^2 \le L_1 L_2$. We can define a coupling coefficient $k = \frac{M}{\sqrt{L_1 L_2}}$. It is evident that $|k| \le 1$. The sign of *k* is indicated by the dots positions. When |*k*| = 1, the magnetic coupling is total. All the magnetic flux generated by one winding flows inside the other one. An extreme case is the ideal transformer.

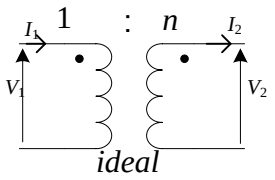


Fig.2- 4 Ideal Transformer

The direction of currents in Fig.2- 4 is non conventional for two port networks. However, it simplifies the analysis of the circuit. *n* is called the turn ratio. The basic equations for the ideal transformer are: $V_2 = nV_1$ and the conservation of power: $V_1 I_1 = V_2 I_2$. Consequently, $I_1 = nI_2$. If we connect a load *Z* at the secondary, it will appear at the primary as $\frac{V_1}{I_1} = \frac{V_1}{V_2}\frac{V_2}{I_2}\frac{I_2}{I_1} = \frac{Z}{n^2}$. This relation can be used for matching impedances. We can also remark that the ideal transformer does not transform the type of impedance. If *Z* is resistive, its transform remains resistive. The same thing results for inductive and capacitive loads. In many cases, the direct use of the circuit of Fig.2- 3 is not very commode. The following one is more useful.

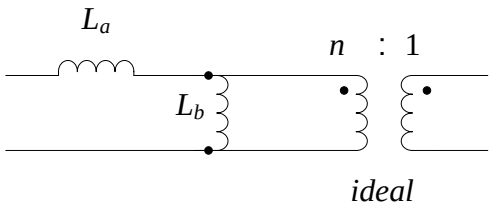


Fig.2- 5 Equivalent circuit

In the above circuit, $L_a = (1 - k^2)L_1$, $L_b = k^2 L_1$ and $n = k\sqrt{\frac{L_1}{L_2}}$. We can remark that *n* has the same sign as *M*. Furthermore, the circuit shows that a physical transformer is equivalent to an ideal transformer if we have total coupling ($k^2 = 1$) and infinite (very large) inductances for the primary (and the secondary) winding. When we have perfect coupling, $n = \pm\sqrt{\frac{L_1}{L_2}}$. We know that the value of an inductance is proportional to the square of the number of turns of its windings. The constant of proportionality depends on its physical size. Since the primary and the secondary are both wound on the same core, we can write $L_1 = \alpha n_1^2$ and $L_2 = \alpha n_2^2$, where n_1 and n_2 are respectively the number of turns of the primary and the secondary. This means that $n = \pm\frac{n_1}{n_2}$ and this justifies the name "turn ratio".

2.4 Parallel RLC circuit

In this section, we are going to analyze a one port network commonly used as a frequency selective filter. This circuit is composed of a resistance R, an inductance L and a capacitance C in parallel.

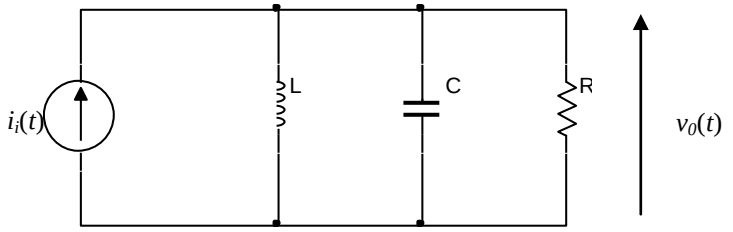


Fig.2- 6 Parallel RLC circuit

The input of the above circuit is a current source. It may represent the collector current of a bipolar transistor for example. The output is the voltage across the parallel RLC circuit[1]. This means that the transfer function is the impedance of the circuit.

$$Z(s) = \frac{1}{\frac{1}{Ls} + Cs + \frac{1}{R}} = \frac{1}{C}\frac{s}{s^2 + \frac{s}{RC} + \frac{1}{LC}}$$

Let $\omega_0^2 = \frac{1}{LC}$ and $2\alpha = \frac{1}{RC} = \frac{\omega_0}{Q_T}$. The transfer function becomes:

[1] Commonly called "Tank" circuit.

$$Z(s) = \frac{1}{C}\frac{s}{s^2 + 2\alpha s + \omega_0^2}$$

This transfer function possesses one zero at the origin and another one at infinity. It has also two poles: $p_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2}$. The poles can be real or complex. Since we use the tank circuit as a narrow bandpass filter, we will consider only the complex case, i.e. $\omega_0 > \alpha$ or $Q_T > \frac{1}{2}$. In this case, we can express the poles as: $p_{1,2} = -\alpha \pm j\beta = -\alpha \pm j\sqrt{\omega_0^2 - \alpha^2}$. Replacing α by its value, we obtain:

$p_{1,2} = -\frac{\omega_0}{2Q_T} \pm j\omega_0\sqrt{1 - \frac{1}{4Q_T^2}}$. If $Q_T > 10$, the poles become $p_{1.2} = -\frac{\omega_0}{2Q_T} \pm j\omega_0$ with a very high precision. In this event, these poles will be also very close to the $j\omega$ axis.

We can remark that the poles satisfy $\omega_0^2 = \alpha^2 + \beta^2$. Given that $\alpha \geq 0$, the locus of the poles in the complex plane is a quarter of a circle on the top left quarter of the plane for one pole and the symmetrical one with respect to the real axis for its conjugate.

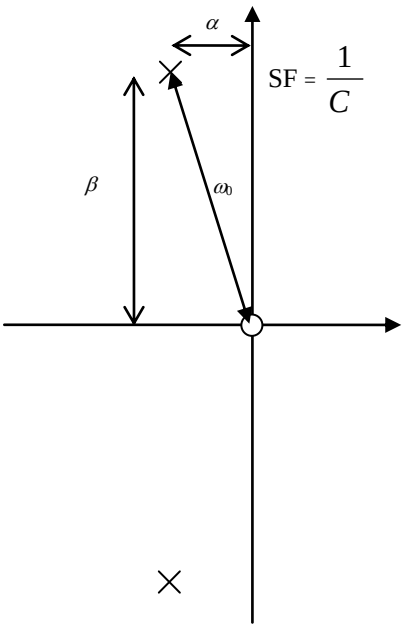


Fig.2- 7 Pole and Zero Plot

The pole and zero plot is a plot of the location of the poles (indicated by ×) and the zeros (indicated by o) along with the value of the scale factor (SF) for a transfer function *H*(*s*):

$$H(s) = SF\frac{(s - z_1)(s - z_2)\cdots(s - z_m)}{(s - p_1)(s - p_2)\cdots(s - p_n)}$$

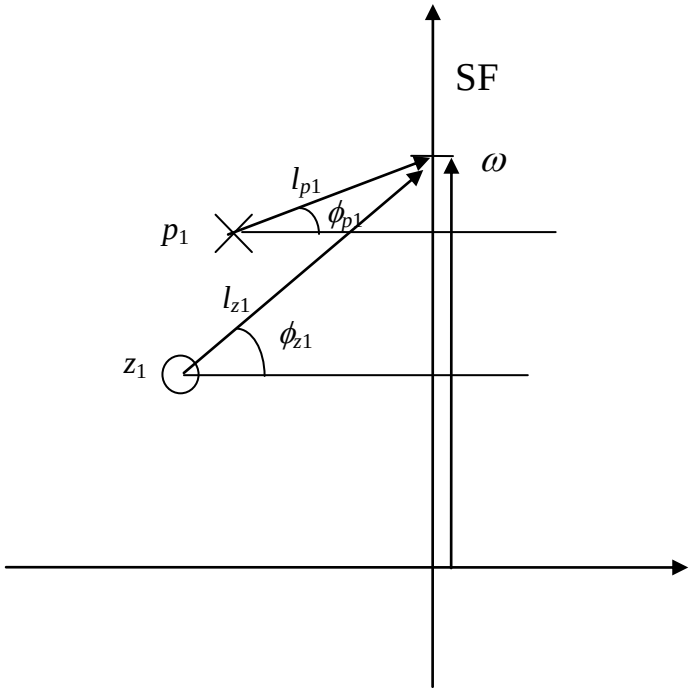


Fig.2- 8 Typical Pole and Zero Plot

The pole and zero plot allows a graphical evaluation of the transfer function in the frequency domain. The transfer function in the frequency domain is the evaluation of $H(s)$ for s on the $j\omega$ axis:

$$H(j\omega) = H(s)\big|_{s=j\omega} = SF\,\frac{(j\omega - z_1)(j\omega - z_2)\cdots(j\omega - z_m)}{(j\omega - p_1)(j\omega - p_2)\cdots(j\omega - p_n)} \tag{1}$$

The modulus and phase versus frequency are given by:

$$|H(j\omega)| = |SF|\,\frac{|j\omega - z_1||j\omega - z_2|\cdots|j\omega - z_m|}{|j\omega - p_1||j\omega - p_2|\cdots|j\omega - p_n|}$$

$$|H(j\omega)| = |SF|\,\frac{l_{z1}l_{z2}\cdots l_{zm}}{l_{p1}l_{p2}\cdots l_{pn}} \tag{2}$$

and $$Arg[H(j\omega)] = Arg[SF] + \sum_{i=1}^{m} Arg[j\omega - z_i] - \sum_{k=1}^{n} Arg[j\omega - p_k]$$

$$Arg[H(j\omega)] = Arg[SF] + \sum_{i=1}^{m} \phi_{zi} - \sum_{k=1}^{n} \phi_{pk} \tag{3}$$

where l_{zi} is the length of the vector joining the zero z_i to the point of coordinate ω on the imaginary axis while ϕ_{zi} is the angle that this vector makes with the real axis. l_{pk} is the length of the vector joining the zero p_k to the point of coordinate ω on the imaginary axis while ϕ_{pk} is the angle that this vector makes with the real axis as shown on Fig.2- 8.

In our case, the existence of a zero at the origin and another one at infinity imply that the value of $|Z(j\omega)|$ at $\omega = 0$ and at $\omega = \infty$ is zero. This means that the

system is bandpass and $|Z(j\omega)|$ is maximum at some frequency. In fact, the pole and zero plot of Fig.2- 7 shows that this frequency is ω_0. We have also $|Z(j\omega_0)| = R$ (at this frequency, the susceptance of L and C cancel each other). In our case, the simple shape of $Z(s)$ allows a straightforward algebraic evaluation of $Z(j\omega)$.

$$Z(j\omega) = \frac{R}{1 + jQ_T \dfrac{\omega^2 - \omega_0^2}{\omega\omega_0}}$$

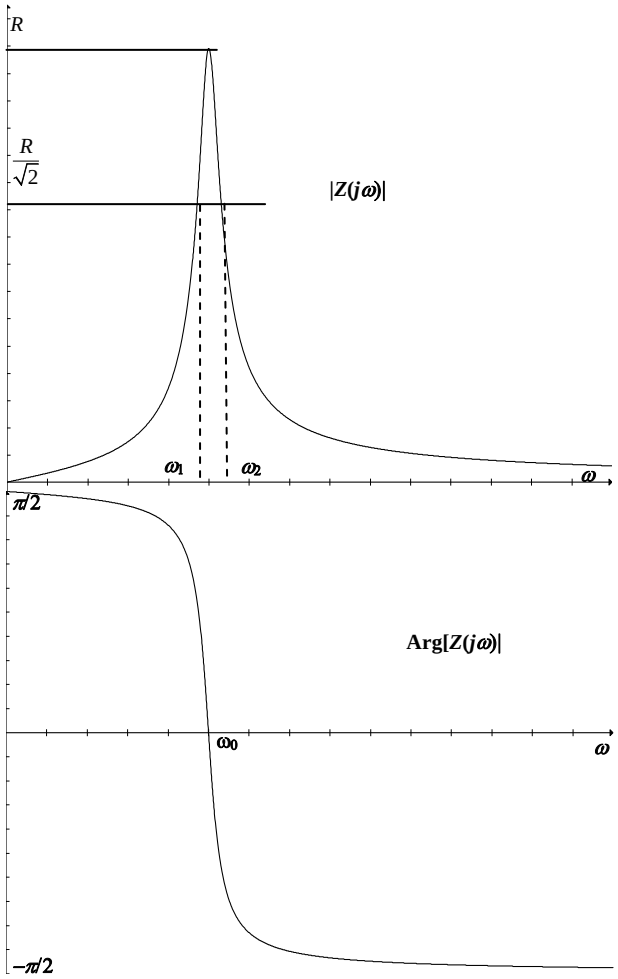


Fig.2- 9 Modulus and Phase Response of the Tank circuit

We remark that the impedance is resistive at $\omega = \omega_0$ (its value is R); it is inductive below ω_0 and capacitive above. From Fig.2- 9, we observe clearly the bandpass nature of the transfer function. The above expression can be used to compute the "3 *dB*" bandwidth of the circuit. The bandwidth B is defined as the difference between the two "3 *dB*" cutoff frequencies: $B = \omega_2 - \omega_1$. These two frequencies are the ones for which $|Z(j\omega_i)| = |Z(j\omega_0)|/\sqrt{2}$, $i = 1,2$. Using the previous equation and solving for ω_1 and ω_2, we obtain:

$$\omega_0 = \sqrt{\omega_1 \omega_2} \text{ and } \omega_2 - \omega_1 = B = \frac{\omega_0}{Q_T}$$

The resonant frequency is the geometric mean of the two cutoff frequencies (it is not in the middle). This result shows clearly that the transfer function is not symmetrical with respect to the resonant frequency. However, when Q_T is high, the two frequencies will become close to each other and the geometric mean will be close to the arithmetic one. This narrow band approximation can be obtained using the technique of graphical evaluation of transfer functions seen previously.

Using the pole and zero plot of Fig.2- 7 and equations (2) and(3), we obtain:

$$|Z(j\omega)| = \frac{1}{C}\frac{l_{z0}}{l_{p1}l_{p2}} \text{ and } Arg[Z(j\omega)] = \phi_{z0} - \phi_{p1} - \phi_{p2}$$

When we evaluate the above equations for ω around ω_0, we obtain:

$l_{z0} = \omega \approx \omega_0$, $l_{p2} \approx 2\omega_0$ because α is very small. So:

$$|Z(j\omega)| \approx \frac{1}{C}\frac{\omega_0}{2\omega_0 l_{p1}} = \frac{1}{2Cl_{p1}}$$

We have also: $\phi_{z0} = \pi/2$, $\phi_{p2} \approx \pi/2$, giving: $Arg[Z(j\omega)] = -\phi_{p1}$. Grouping the two results, we finally get:

$$Z(j\omega) \approx \frac{1}{2Cl_{p1}e^{j\phi_{p1}}}$$

The complex number $l_{p1}e^{j\phi_{p1}}$ is the vector connecting the pole p_1 to the point $j\omega$ in the complex plane. So,

$$l_{p1}e^{j\phi_{p1}} = j\omega - (-\alpha + j\beta) = \alpha + j(\omega - \beta) \approx \alpha + j(\omega - \omega_0).$$

This implies that we can approximate $Z(j\omega)$ very closely by:

$$Z(j\omega) \approx \frac{1}{2C[\alpha + j(\omega - \omega_0)]} = \frac{1}{2C\alpha}\frac{1}{1 + j\frac{\omega - \omega_0}{\alpha}} = \frac{R}{1 + j2Q_T\frac{\omega - \omega_0}{\omega_0}} \quad (4)$$

The above result is valid for positive frequencies around ω_0. For negative frequencies, we can use the fact that $Z(j\omega) = Z^*(-j\omega)$. Fig.2- 10 (for $Q_T = 10$, $\omega_0 = 5$ rd/s and $R = 10\ \Omega$) shows that the two responses are very close. In fact, the approximation is very accurate for all frequencies between the cutoff frequencies ω_1 and ω_2. A closer look at the approximation shows that the curve is symmetrical with respect to the line $\omega = \omega_0$. In fact, the resonant frequency is now the middle of the interval [ω_1, ω_2]. Equation (4) is commonly used when we want to obtain the equivalent lowpass filter for the analysis of bandpass signals.

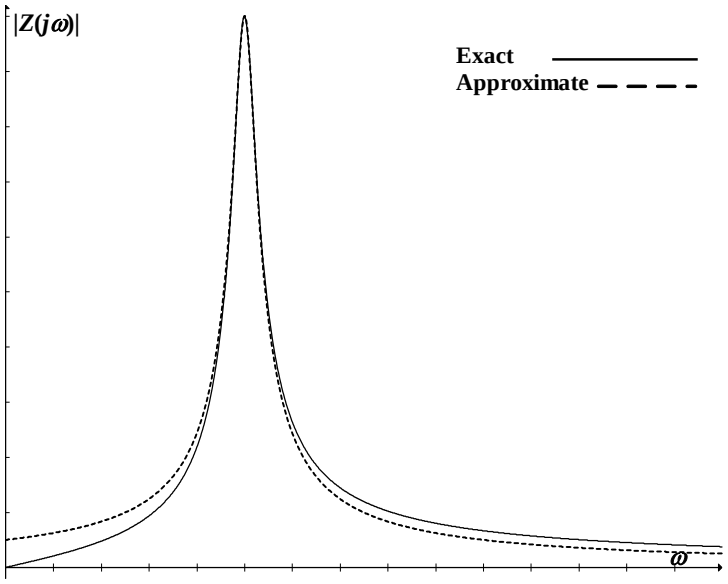


Fig.2- 10 Exact and Approximate Amplitude response

2.5 Series Resonant Circuit

When the signal source has low impedance, it is usually modeled as an ideal voltage source. At that time, we cannot use a parallel tank circuit since any circuit in parallel with an ideal voltage source will have no effect. A series resonant circuit corresponds to the circuit shown below.

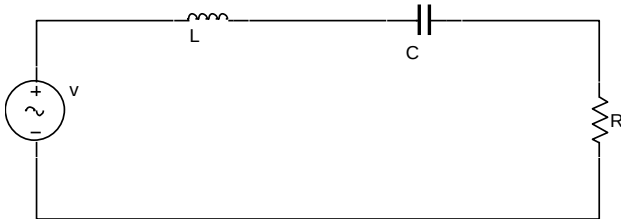


Fig.2- 11 Series Resonant Circuit

We don't have to repeat the analysis for the above circuit. By using the principle of duality, we can immediately derive the admittance function of the circuit. We simply replace *L* by *C*, *C* by *L*, *R* by *G*, *Z* by *Y* and *i* by *v*.

The parallel tank circuit had an impedance function given by:

$$Z(s) = \frac{1}{C} \frac{s}{s^2 + \frac{s}{RC} + \frac{1}{LC}}$$

The application of the duality principle gives:

$$Y(s) = \frac{1}{L} \frac{s}{s^2 + \frac{s}{LG} + \frac{1}{LC}} = \frac{1}{L} \frac{s}{s^2 + \frac{R}{L}s + \frac{1}{LC}}$$

Having the same transfer function, the analysis of this circuit will be identical to the one derived for the parallel RLC circuit and is left as an exercise.

2.6 Parallel Resonant Circuit with Series Loss

If one of the reactive elements in a parallel connection of an inductor and a capacitor possesses series loss, the zeroes of the impedance function are going to move. If the loss is in series with the capacitor, the zero at infinity moves to a finite value.

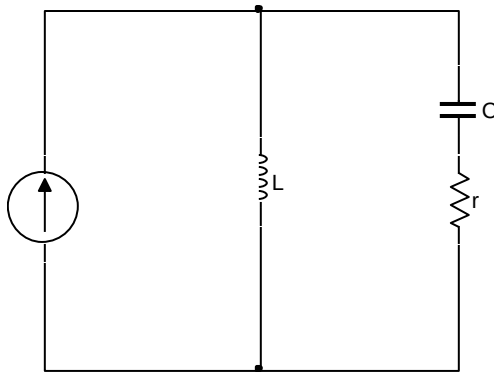


Fig.2- 12 Parallel Resonant Circuit with Series Loss

The impedance transfer function in this case is given by the parallel combination of the inductance L and the series arrangement of the capacitance and resistance. So:

$$Z(s) = \frac{Ls\left(r + \frac{1}{Cs}\right)}{Ls + r + \frac{1}{Cs}} = \frac{rs\left(s + \frac{1}{rC}\right)}{s^2 + \frac{r}{L}s + \frac{1}{LC}}$$

Let $\alpha = \frac{r}{2L}$, $\omega_0^2 = \frac{1}{LC}$ and $Q_C = \frac{1}{rC\omega_0}$. The impedance transfer function has two real zeros: at the origin and at $-\frac{1}{rC}$. It has two poles: at $-\alpha \pm j\beta = -\alpha \pm j\sqrt{\omega_0^2 - \alpha^2}$.

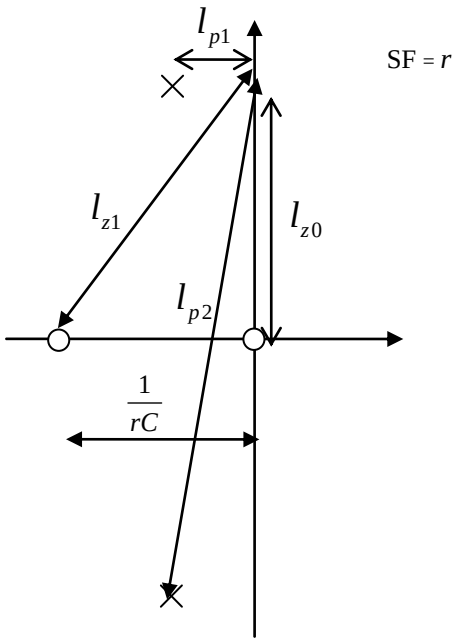


Fig.2- 13 Pole and Zero Plot

According to the above pole and zero plot, if α is small, the two poles will be complex and their imaginary part β will be practically ω_0. A simple manipulation shows that $\alpha = \frac{\omega_0}{2Q_C}$. The fact that this transfer function has two zeros and two poles implies that the value of the impedance at infinity is different from zero. In fact $Z(\infty) = r$. From the pole and zero plot, we also have:

$$|Z(j\omega_0)| = \frac{r l_{z0} l_{z1}}{l_{p1} l_{p2}}$$

along with: $l_{z0} = \omega_0$, $l_{z1} = \sqrt{\frac{1}{r^2C^2} + \omega_0^2}$, $l_{p1} = \frac{r}{2L}$ and $l_{p2} \approx 2\omega_0$. This gives: $|Z(j\omega_0)| \approx L\omega_0\sqrt{1+Q_C^2}$. We also have $L\omega_0 = rQ_C$. So, $|Z(j\omega_0)| \approx rQ_C\sqrt{1+Q_C^2}$. If $Q_C > 10$, $|Z(j\omega_0)| \approx rQ_C^2$. It is also apparent from the same pole and zero plot that $Arg[Z(j\omega_0)] \approx 0$ if $Q_C > 10$. Then, we can say that if $Q_C > 10$, the impedance of the circuit at ω_0 is resistive and is equal to:

$$R = rQ_C^2 \qquad (5)$$

For all frequencies around ω_0, the circuit is equivalent to a parallel RLC circuit. Equation (5) can be used for impedance transformation (matching). For the high Q case and if r is small, we can say that most of the time $|s|$ can be neglected compared with $\frac{1}{rC}$. The transfer function becomes:

$$Z(s)=\frac{rs\left(\frac{1}{rC}\right)}{s^2+2\alpha s+\omega_0^2}=\frac{1}{C}\frac{s}{s^2+2\alpha s+\omega_0^2}$$

Using (5), we can see that $Q_C=\frac{1}{rC\omega_0}=RC\omega_0$ and that $\alpha=\frac{1}{2RC}$. This is the same as the one of the parallel RLC circuit.

If now the loss is in series with the inductor, the same analysis can be repeated, but now it is the zero at the origin that moves to a real negative value.

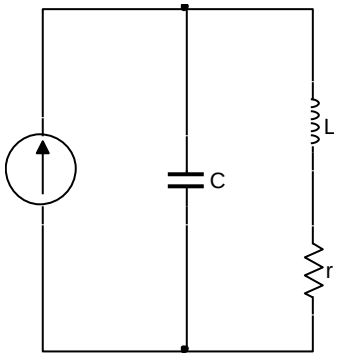


Fig.2- 14 Inductor with series loss

$$Z(s)=\frac{\frac{1}{Cs}(r+Ls)}{\frac{1}{Cs}+r+Ls}=\frac{1}{C}\frac{\left(s+\frac{r}{L}\right)}{s^2+\frac{r}{L}s+\frac{1}{LC}}$$

In this case also, if $Q_L=\frac{L\omega_0}{r}\geq 10$, then we can replace the series circuit composed of r and L by a parallel one composed of L in parallel with $R=Q_L^2 r$. Both circuits can be used for impedance matching. The value of Q is used to transform a small resistive load to a large apparent load. So, in this part, we find the same results as the ones derived in the series parallel transformations. To see an example of application, refer to the example in page 31.

2.7 Transformer like networks

The matching networks described above allow impedance transformation at a single frequency. However, their frequency response around that frequency is not very accurate. They are bandpass, but since they are built around only two components (a capacitance and an inductance), we have only two degrees of freedom. We can set the resonant frequency and the impedance transformation. The impedance transformation is due to a multiplication by Q^2. This fixes the value of the bandwidth. In general, we need circuits that have three degrees of

freedom if we want to set three quantities: The impedance transformation, the resonant frequency and the 3 dB bandwidth. One solution is to use a tank circuit in cascade with an ideal transformer.

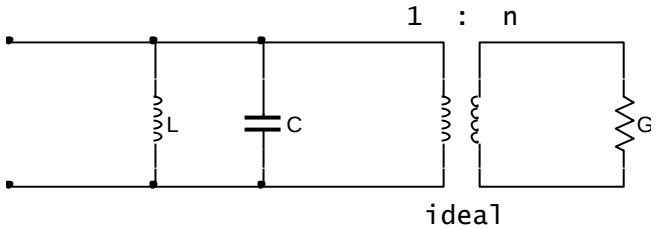


Fig.2- 15 Ideal transformer matching

In the above circuit the conductance is reflected to the input of the transformer to a value equal to n^2G. The resonant frequency is given by $\omega_0^2 = \frac{1}{LC}$ and the quality factor is $Q = \frac{\omega_0 C}{n^2 G}$. So, we have three elements that can be adjusted in order to set the above cited three parameters. The ideal transformer can be approximated by a transformer wound around a toroidal core such as the ones illustrated below.

Fig.2- 16 Toroidal core transformers

The problem with these transformers is that they are rather bulky and if we have to use them, they are quite far from ideal. We are going to analyze circuits that have the same behavior but that do not use ideal transformer.

The first system is a split capacitor network.

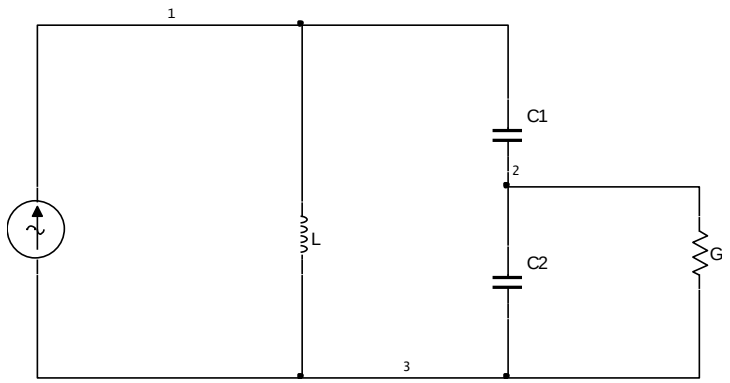


Fig.2- 17 Split capacitor matching network

Under circumstances that will be stated later, this circuit is equivalent to the one shown in Fig.2- 15. To show this equivalence, we have to show that the two circuits have the same input impedance (loaded) and the same transfer function.

The input impedance of the circuit is given by:

$$Z_{11}(s) = \frac{1}{\frac{1}{Ls} + \frac{1}{\frac{1}{C_1 s} + \frac{1}{C_2 s + G}}} = \frac{1}{C} \frac{s\left(s + \frac{G}{C_1 + C_2}\right)}{s^3 + \frac{G}{C_2} s^2 + \frac{1}{LC} + \frac{G}{LC_1 C_2}}$$

where C is the series equivalent capacitance of C_1 and C_2: $C = \frac{C_1 C_2}{C_1 + C_2}$.

We see that $Z_{11}(s)$ has two finite real zeroes (at the origin and at $-\frac{G}{C_1 + C_2}$) and three poles. One pole is always real; the other two can be either real or complex conjugate. In order for the system to be narrow band bandpass, the poles must be complex at $-\alpha \pm j\beta$. The denominator can then be written as:

$$(s + \gamma)(s + \alpha + j\beta)(s + \alpha - j\beta)$$

The pole and zero plot is shown in Fig.2- 18. If we want to have equivalence with a parallel RLC circuit, we must have a cancellation between the real pole at $-\gamma$ and the real zero at $-\frac{G}{C_1 + C_2}$. To find conditions for this to occur, let us identify the development of the denominator in terms of α, β and γ and the one in terms of G, L, C_1 and C_2.

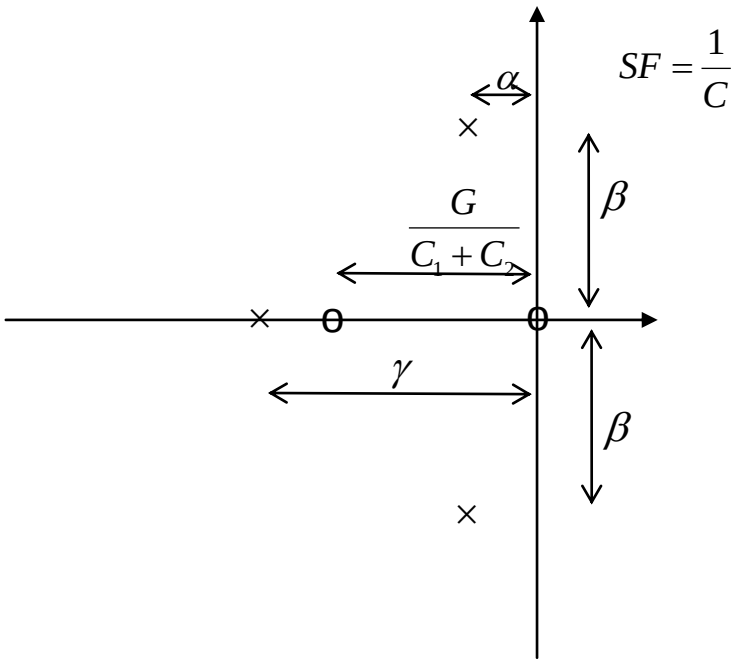


Fig.2- 18 Pole and Zero Plot

Developing the denominator, we obtain:

$$s^3 + (\gamma + 2\alpha)s^2 + (\alpha^2 + \beta^2 + 2\alpha\gamma)s + \gamma(\alpha^2 + \beta^2)$$

Identifying the coefficients in the two polynomials produce the following three equations:

$$\gamma + 2\alpha = \frac{G}{C_2}$$

$$\alpha^2 + \beta^2 + 2\alpha\gamma = \frac{1}{LC} \equiv \omega_0^2$$

$$\gamma(\alpha^2 + \beta^2) = \frac{G}{LC_1C_2}$$

We know that in the impedance function of the parallel RLC circuit, the root locus of the complex poles is a circle of radius ω_0, i.e. $\alpha^2 + \beta^2 = \omega_0^2$. So, we can rewrite the second equation as follows:

$\alpha^2 + \beta^2 = \omega_0^2\left(1 - \frac{2\alpha\gamma}{\omega_0^2}\right)$ in order to be able to appreciate the precision of the approximation (in percent). Let us call $\Omega = \frac{\omega_0^2}{2\alpha\gamma}$. The three equations are then:

$$2\alpha = \frac{n^2 G}{C}\left(\frac{1-\frac{1}{n\Omega}}{1-\frac{1}{\Omega}}\right)$$

$$\alpha^2 + \beta^2 = \omega_0^2\left(1-\frac{1}{\Omega}\right)$$

$$\gamma = \frac{G}{C_1 + C_2}\frac{1}{1-\frac{1}{\Omega}}$$

where $n = \frac{C_1}{C_1 + C_2}$.

Now, if Ω > 100, we have $\gamma \approx \frac{G}{C_1 + C_2}$ with an error that is less than 1% and of course $\alpha^2 + \beta^2 \approx \omega_0^2$. The real part of the poles satisfies:

$$2\alpha \approx \frac{n^2 G}{C}\left(1-\frac{1}{n\Omega}\right)$$

Even if Ω is larger than 100, we cannot eliminate the product $n\Omega$ because n is less than 1. So, if Ω is larger than 100, we have the pole and zero cancellation and the input impedance will be the one of a parallel RLC circuit.

$$Z_{11}(s) \approx \frac{1}{C}\frac{s}{s^2 + 2\alpha s + \omega_0^2}$$

So, if we can control the value of Ω, we can find conditions for the equivalence. The problem is that Ω does not correspond to physical quantities. In order to have criteria that depend directly on the circuit elements, let us develop the expression of Ω.

$$\Omega = \frac{\omega_0^2}{2\alpha\gamma} = \omega_0^2 \frac{C\left(1-\frac{1}{\Omega}\right)}{n^2 G\left(1-\frac{1}{n\Omega}\right)}\frac{\left(C_1 + C_2\right)\left(1-\frac{1}{\Omega}\right)}{G}$$

We can introduce two "Que's":

$$Q_{T'} = \frac{\omega_0 C}{n^2 G} \text{ and } Q_E = \frac{\omega_0\left(C_1 + C_2\right)}{G}.$$

$Q_{T'}$ corresponds to the Q of a tank circuit composed of the capacitance C in parallel with the inductance L and in parallel with $R_{T'} = \frac{1}{n^2 G}$. Q_E on the other hand corresponds to the Q of the parallel combination of G with C_1 and C_2.

The expression of Ω becomes:

$$\Omega = \frac{Q_T Q_E \left(1-\frac{1}{\Omega}\right)^2}{\left(1-\frac{1}{n\Omega}\right)} \text{ giving } \Omega - \frac{1}{n} = Q_T Q_E \left(1-\frac{1}{\Omega}\right)^2$$

So if Ω is large, then we obtain: $\Omega \approx Q_T Q_E + \frac{1}{n}$.

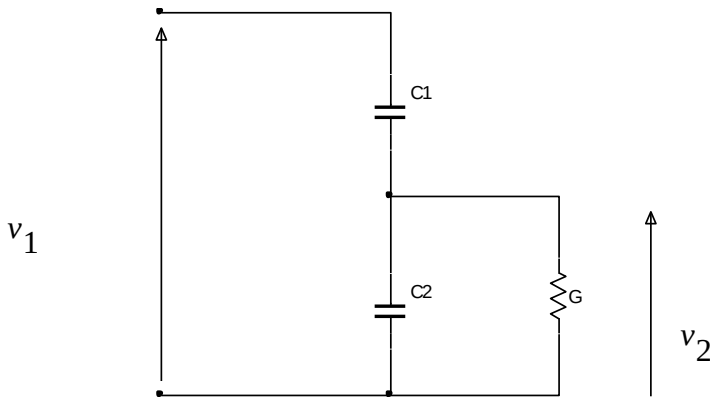
The above expression shows clearly that, if $Q_T Q_E > 100$, then Ω will be even larger. At that time, from the input impedance point of view, the circuit becomes equivalent to a resistance R_T in parallel with C in parallel with L where:

$$G_T = \frac{1}{R_T} = n^2 G\left(1-\frac{1}{nQ_T Q_E + 1}\right) \quad (6)$$

However, if $nQ_T Q_E > 100$, then $G_T = \frac{1}{R_T} = n^2 G$.

Under the above condition, the circuit is then equivalent to the circuit shown in Fig.2- 15. To have the complete equivalence, we must show that the voltage transfer of the circuit is the one of the ideal transformer. In other words, the voltage transfer of the circuit must be $H(s) \approx n$.

H(s) is the transfer of the following voltage divider:



$$H(s) = \frac{C_1}{C_1 + C_2} \frac{s}{s + \frac{G}{C_1 + C_2}}$$

Evaluating the above expression on the imaginary axis provides:

$$H(j\omega) = n\frac{j\frac{\omega}{\omega_0}}{j\frac{\omega}{\omega_0}+\frac{1}{Q_E}}$$

So, if $Q_E > 10$, we can safely say that $H(j\omega) \approx n$ at all frequencies. To resume the different approximations, we can say that if $Q_{T'}Q_E > 100$, the split capacitor circuit is equivalent to a parallel tank circuit loaded by a resistance given by equation (6). If we have $nQ_{T'}Q_E > 100$, the circuit is equivalent to the circuit shown in Fig.2- 15, but only from the input impedance point of view. If we add the condition $Q_E > 10$, the equivalence becomes complete and we can replace the circuit of Fig.2- 17 by the one of Fig.2- 15. This approximation will greatly simplify the analysis of circuits.

In the next circuit, we use a voltage divider built by means of two inductors.

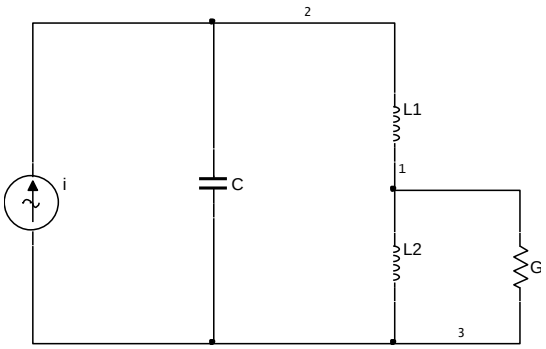


Fig.2- 19 Split Inductance Circuit

In the circuit shown above, we assume that there is no magnetic coupling between the two inductances. We don't have to redo the same analysis for this circuit. The tank circuit resonant frequency is $\omega_0 = \frac{1}{\sqrt{LC}}$. L is the inductance of the series connection of the two inductances L_1 and L_2, $L = L_1 + L_2$. The ideal transformer turn ratio n is the voltage transfer of the circuit with no load (G = 0). So, $n = \frac{L_2}{L_1 + L_2}$. Applying the definitions of $Q_{T'}$ and Q_E given previously we get:

$Q_{T'} = \frac{\omega_0 C}{n^2 G}$ (Q of a tank circuit composed of the capacitance C in parallel with the inductance L and in parallel with $R_{T'} = \frac{1}{n^2 G}$) and $Q_E = \frac{L_1 + L_2}{L_1 L_2 \omega_0 G}$ (Q of the parallel combination of G with L_1 and L_2).

If there exist magnetic coupling between the inductors, we obtain a transformer.

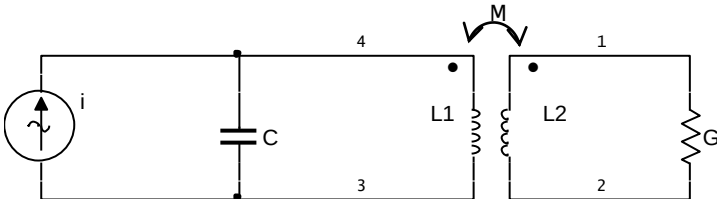
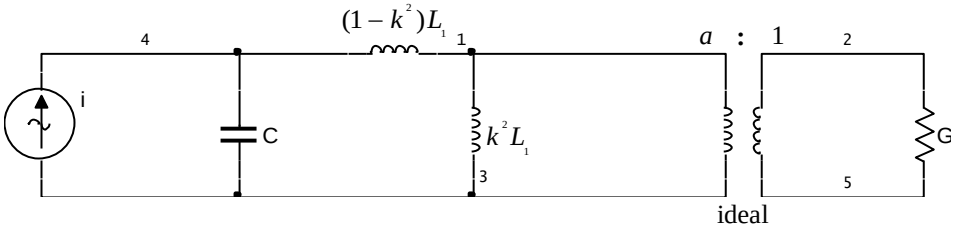


Fig.2- 20 Tuned Primary Transformer

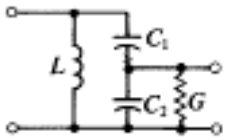
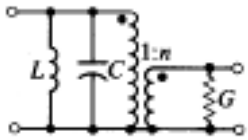
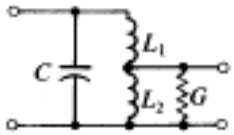
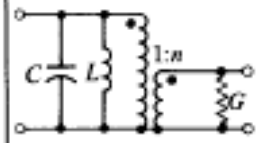
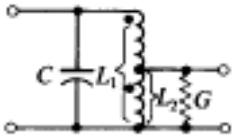
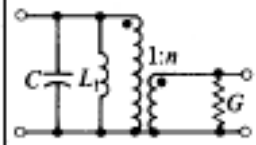
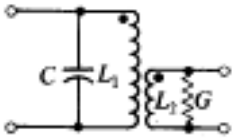
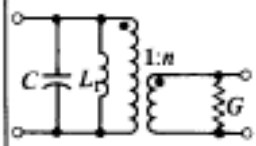
Using the equivalence derived in (2.3 Mutual Inductance and transformer), we can replace the transformer composed of L1, L2 and M by the equivalent circuit shown in Fig.2- 5, we obtain the following circuit.



It corresponds to the split inductor circuit loaded by a conductance $\frac{G}{a^2}$, where a is the turn ratio of the ideal transformer. The coupling coefficient k is given by $k = \frac{M}{\sqrt{L_1 L_2}}$ and the turn ratio a is given by $a = k\sqrt{\frac{L_1}{L_2}}$. The turn ratio of the ideal transformer corresponding to the split inductor is $n' = \frac{k^2 L_1}{(1-k^2)L_1 + k^2 L_1} = k^2$ and the series combination of the two inductances is $L = L_1$. The final equivalence is a cascade of two transformers corresponding to a single transformer with turn ratio $n = \frac{n'}{a} = k\sqrt{\frac{L_2}{L_1}}$. Replacing $k = \frac{M}{\sqrt{L_1 L_2}}$ we obtain $n = \frac{M}{L_1}$; $Q_{T'} = \frac{\omega_0 C}{n'^2 G'} = \frac{\omega_0 C}{nG}$ and $Q_E = \frac{1}{L_1(1-k^2)n^2 G\omega_0}$.

If the transformer is tightly coupled ($|k| \approx 1$), Q_E will be very large and the equivalence with the ideal transformer is always valid. The above analysis can also be extended to the autotransformer.

The following table is taken from the textbook and summarizes the different conditions for equivalence for all circuits.

Circuit	Model for determining $Z_{11}(p)$ and $Z_{12}(p)$	n	ω_0	Q_T	Q_E	Limitations for $Z_{11}(p)$: $n'Q_T$, $Q_E > 100$ Limitations for $Z_{12}(p)$: $n'Q_T$, $Q_E > 100$ and $Q_E > 10$
	 $C = \frac{C_1 C_2}{C_1 + C_2}$	$\frac{C_1}{C_1+C_2}$ $n'=n$	$\frac{1}{\sqrt{LC}}$	$\frac{\omega_0 C}{n^2 G}$	$\frac{\omega_0(C_1+C_2)}{G}$	
	 $L = L_1 + L_2$	$\frac{L_2}{L_1+L_2}$ $n'=n$	$\frac{1}{\sqrt{LC}}$	$\frac{\omega_0 C}{n^2 G}$	$\frac{L_1+L_2}{\omega_0 L_1 L_2 G}$	
		$\frac{M}{L_1}$ $n'=k^2$	$\frac{1}{\sqrt{L_1 C}}$	$\frac{\omega_0 C}{n^2 G}$	$\frac{1}{\omega_0 L_1(1-k^2)G}$	
		$\frac{M}{L_1}$ $n'=k^2$	$\frac{1}{\sqrt{L_1 C}}$	$\frac{\omega_0 C}{n^2 G}$	$\frac{1}{\omega_0 L_1(1-k^2)G}$	

Except for the transformer based circuits, the previous networks are step down. The equivalent turn ratio is always less than one. The next circuit, on the other hand, is step up. In fact, it is a split capacitor circuit used in reverse.

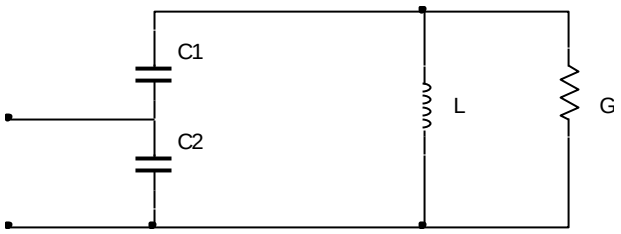


Fig.2- 21 Step Up Transformer

The input impedance is:

$$Z_{in} = \frac{1}{C_2 s + \frac{1}{\frac{1}{C_1 s} + \frac{1}{G + \frac{1}{Ls}}}}$$

After simplification, we obtain:

$$Z_{in} = \frac{1}{C_2 s} \frac{s^2 + \frac{G}{C_1} s + \frac{1}{LC_1}}{s^2 + \frac{G}{C} s + \frac{1}{LC}}$$

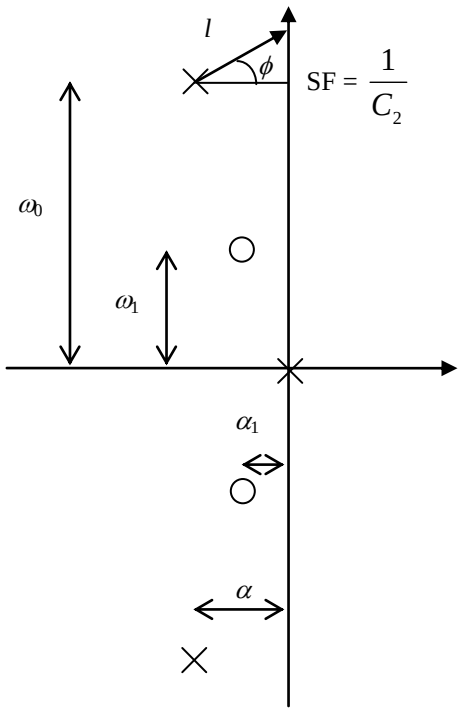
with $C = \frac{C_1 C_2}{C_1 + C_2}$. Replacing $\omega_0^2 = \frac{1}{LC}$, $\omega_1^2 = \frac{1}{LC_1}$, $\alpha = \frac{G}{2C}$ and $\alpha_1 = \frac{G}{2C_1}$, we obtain:

$$Z_{in} = \frac{1}{C_2 s} \frac{s^2 + 2\alpha_1 s + \omega_1^2}{s^2 + 2\alpha s + \omega_0^2}$$

There are two finite zeros and 3 poles:

$z_{1,2} = -\alpha_1 \pm j\sqrt{\omega_1^2 - \alpha_1^2}$ and $p_0 = 0$, $p_{1,2} = -\alpha \pm j\sqrt{\omega_0^2 - \alpha^2}$

We assume that the zeros and the poles are complex. We obtain the following pole & zero plot:



An exact analysis (like the previous case) cannot be performed. The next analysis is thus valid for the high Q case.

Since $C < C_1$, we have $\omega_0 > \omega_1$ and $\alpha > \alpha_1$. If we assume that we operate only around ω_0, then, if α is very small, we can write:

$|Z_{in}| \simeq \frac{1}{C_2} \frac{(\omega_0 - \omega_1)(\omega_0 + \omega_1)}{\omega_0 \times 2\omega_0 \times l}$ and $\text{Arg}[Z_{in}] \simeq -\phi$ giving: $Z_{in} \simeq \frac{1}{2C_2} \frac{\omega_0^2 - \omega_1^2}{\omega_0^2} \frac{1}{le^{j\phi}}$

$le^{j\phi}$ is the vector represented in the above figure joining the point $-\alpha + j\omega_0$ to the point $j\omega$ in the s-plane. Using the definition of ω_0 and ω_1, we obtain:

$\frac{\omega_0^2 - \omega_1^2}{\omega_0^2} = 1 - \frac{C}{C_1}$. Let $n = \frac{C_1}{C_1 + C_2}$, then $C_2 = \frac{C}{n}$ and $C_1 = \frac{C}{1-n}$ and finally: $\frac{\omega_0^2 - \omega_1^2}{\omega_0^2} = n$. So: $Z_{in} = \frac{n}{2C_2\alpha} \frac{1}{1 + j\frac{(\omega - \omega_0)}{\alpha}}$. The final result is:

$$Z_{in} = \frac{n^2}{G} \frac{1}{1 + j\frac{(\omega - \omega_0)}{\alpha}}$$

and for frequencies ω around ω_0, the circuit is equivalent to the following figure for the input impedance point of view.

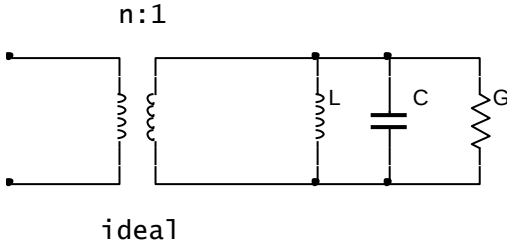


Fig.2- 22 Step Up equivalent circuit

To obtain a complete equivalence, the voltage transfer of the circuit must be the one of the ideal transformer. The voltage transfer is given by:

$$H(s) = \frac{s^2}{s^2 + 2\alpha_1 + \omega_1^2}$$

Under the same previous hypotheses, we obtain:

$|H| \simeq \frac{\omega_0^2}{\omega_0^2 - \omega_1^2} = \frac{1}{n}$ and $Arg[H] \simeq 0$ for frequencies around ω_0.

This approximate analysis is valid for bandlimited signals and for $Q = \frac{\omega_0 C}{G} > 10$. The bandwidth of the signals must be much smaller than $2(\omega_0 - \omega_1)$ in order to remain always in the vicinity of the pole.

The final transformer like network is the "pi" circuit. This circuit is commonly used in power amplifiers. We will not make a complete analysis of the circuit. The advantage of the "pi" circuit is that it can be used either as a step up or as a step down transformer.

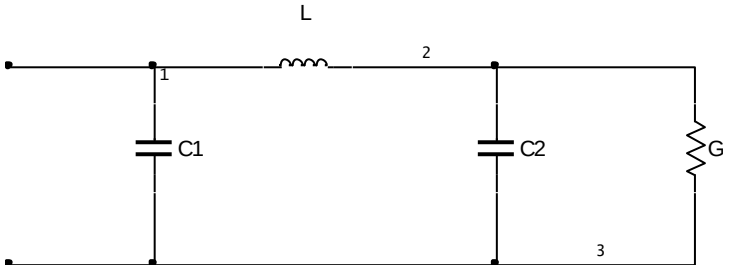


Fig.2- 23 The Pi Network

In this case also, we are going to study the input impedance and the transfer function. The input impedance is given by:

$$Z_{11}(s)=\frac{1}{C_1 s+\frac{1}{Ls}+\frac{1}{C_2 s+G}}=\frac{1}{C_1}\frac{s^2+\frac{G}{C_2}s+\frac{1}{LC_2}}{s^3+\frac{G}{C_2}s^2+\frac{C_1+C_2}{LC_1C_2}s+\frac{G}{LC_1C_2}}$$

Introducing: $C=\frac{C_1C_2}{C_1+C_2}$; $\omega_0^2=\frac{1}{LC}$; $\omega_2^2=\frac{1}{LC_2}$; $Q_2=\frac{\omega_0 C_2}{G}$ and $N=\frac{C_2}{C_1}$, the input impedance is expressed as:

$$Z_{11}(s)=\frac{1}{C_1}\frac{s^2+\frac{\omega_0}{Q_2}s+\omega_2^2}{s^3+\frac{\omega_0}{Q_2}s^2+\omega_0^2 s+\frac{N\omega_0\omega_0^2}{Q_2}}$$

This function has two finite zeroes. If Q_2 is large enough, these zeroes are complex:

$$z_{1,2}=-\frac{\omega_0}{2Q_2}\pm j\sqrt{\omega_2^2-\frac{\omega_0^2}{4Q_2^2}}\,.$$

It has three poles: at $-\gamma$ and at $-\alpha\pm j\beta$.

Using the same technique as for the split capacitor, we obtain the following three equations:

$$2\alpha+\gamma=\frac{\omega_0}{Q_2}$$

$$\alpha^2+\beta^2+2\alpha\gamma=\omega_0^2$$

$$\left(\alpha^2+\beta^2\right)\gamma=\frac{N\omega_0\omega_2^2}{Q_2}$$

In this case also we introduce the variable $\Omega=\frac{\omega_0^2}{2\alpha\gamma}$. The above three equations become:

$$2\alpha=\frac{\omega_0}{(N+1)Q_2}\frac{1-\frac{N+1}{\Omega}}{1-\frac{1}{\Omega}}$$

$$\alpha^2+\beta^2=\omega_0^2\left(1-\frac{1}{\Omega}\right)$$

$$\gamma=\frac{N\omega_2^2}{Q_2\omega_0}\frac{1}{1-\frac{1}{\Omega}}$$

If $\Omega>100$, we obtain the following equations:

$$\alpha^2+\beta^2\simeq\omega_0^2$$

$$\gamma\simeq\frac{N\omega_2^2}{Q_2\omega_0}$$

$$2\alpha\simeq\frac{\omega_0}{Q_2(N+1)}\left(1-\frac{N+1}{\Omega}\right)$$

Replacing the expressions of α and γ in the definition of Ω, we obtain:

$$\Omega-(N+1)=\frac{\omega_0^2Q_2^2(N+1)}{\omega_2^2N}\left(1-\frac{1}{\Omega}\right)^2$$

We also have $\frac{\omega_2^2}{\omega_0^2}=\frac{1}{N+1}$. So, when Ω is large, we obtain:

$$\Omega\approx\frac{(N+1)^2}{N}Q_2^2+N+1$$

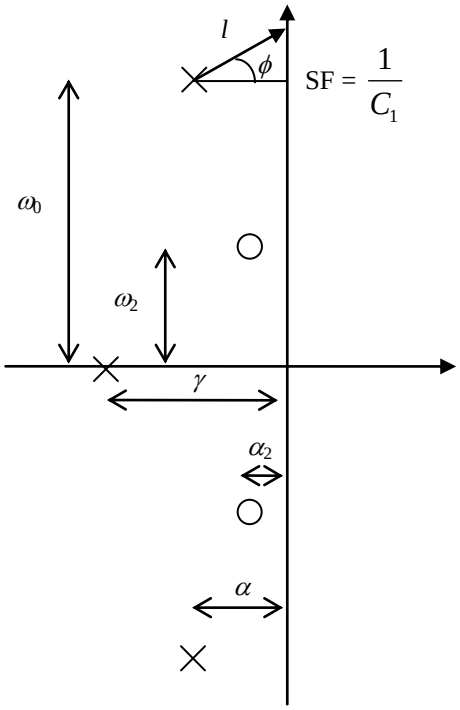
So, if $Q_2>10$, $\Omega>100$. Furthermore, if $Q_2\sqrt{\frac{N+1}{N}}>10$, $\frac{\Omega}{N+1}>100$. At that time:

$$\alpha^2 + \beta^2 \simeq \omega_0^2$$

$$\gamma \simeq \frac{N\omega_2^2}{Q_2\omega_0}$$

$$2\alpha \simeq \frac{\omega_0}{Q_2(N+1)}$$

In order to progress in our analysis, we must resort to narrowband analysis. It is not possible to obtain a more general result. The following figure shows the pole and zero plot.



Using the above plot, we obtain: for ω around ω_0

$$|Z_{11}(j\omega)| \approx \frac{1}{C_1}\frac{(\omega_0+\omega_2)(\omega_0-\omega_2)}{2\omega_0^2 l} = \frac{1}{C_1}\frac{\omega_0^2-\omega_2^2}{2\omega_0^2 l}$$

The argument is practically $-\phi$. Given that $le^{j\phi} = j\omega - (-\alpha + j\omega_0) = \alpha + j(\omega - \omega_0)$, the expression of the impedance becomes:

$$Z_{11}(j\omega) \approx \frac{1}{C_1}\frac{\omega_0^2-\omega_2^2}{2\omega_0^2(\alpha + j(\omega-\omega_0))}$$

Replacing $\omega_2^2 = \frac{\omega_0^2}{N+1}$ and $2\alpha = \frac{\omega_0}{Q_2(N+1)}$, we obtain the following expression:

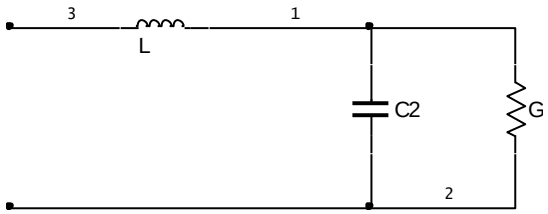
$$Z_{11}(j\omega) \approx \frac{NQ_2}{C_1\omega}\frac{1}{1+j\frac{\omega-\omega_0}{\alpha}}$$

Since $Q_2 = \frac{\omega_0 C_2}{G}$, the final result is:

$$Z(j\omega) \approx \frac{N^2}{G} \frac{1}{1 + j\frac{\omega - \omega_0}{\alpha}}$$

So, from the input impedance point of view, the impedance is the same as the one of a parallel tank circuit loaded by a resistance of value $\frac{N^2}{G}$.

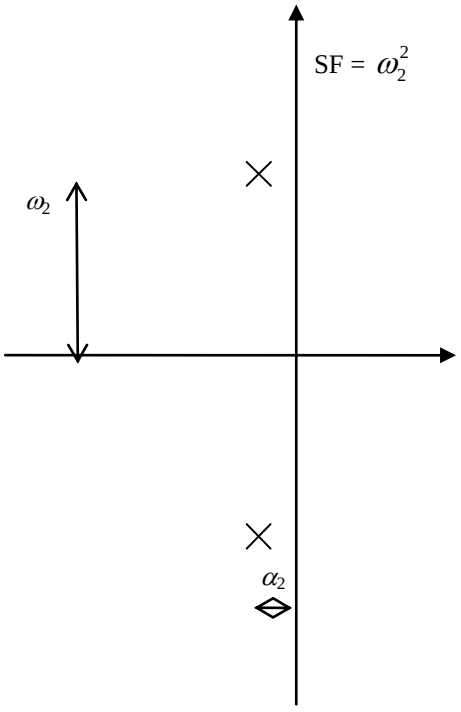
The transfer function is the transfer of the following voltage divider:



The transfer function is:

$$H(s) = \frac{\frac{1}{C_2 s + G}}{Ls + \frac{1}{C_2 s + G}} = \frac{\omega_2^2}{s^2 + \frac{\omega_0}{Q_2} s + \omega_2^2}$$

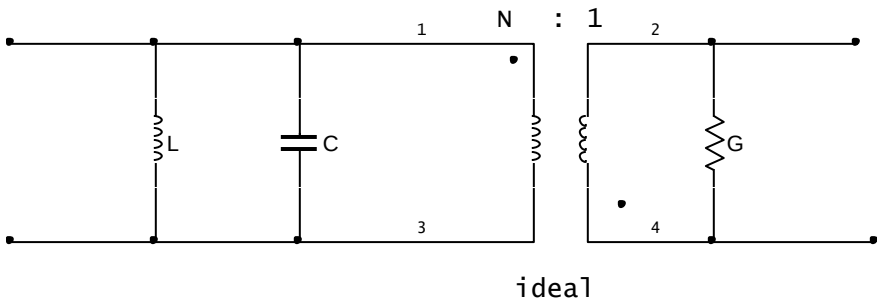
Using a narrowband approximation and operating at a frequency around ω_0, we obtain from the following pole and zero plot:



$$|H(j\omega)| \approx \frac{\omega_2^2}{(\omega_0+\omega_2)(\omega_0-\omega_2)} = \frac{\omega_2^2}{\omega_0^2-\omega_2^2} = \frac{1}{N}$$

and $$\arg[H(j\omega)] \approx \frac{\pi}{2} + \frac{\pi}{2} = \pi$$

So for the stated conditions: $Q_2\sqrt{\frac{N+1}{N}} > 10$ and narrowband signals operating around ω_0, the pi network is equivalent to:



Response of a tank circuit to a periodic input

If we apply a periodic signal to a parallel RLC circuit, its response will be also periodic, but with harmonics that will be much reduced. Consider the following periodic current:

$$i(t) = \sum_{n=0}^{\infty} I_n \cos n\omega_0 t$$

applied to a parallel RLC network tuned at ω_0. The voltage across the tank circuit is given by:

$$v(t) = \sum_{n=1}^{\infty} |Z(jn\omega_0)| I_n \cos\left(n\omega_0 t + \arg[Z(jn\omega_0)]\right)$$

If the Q of the tank circuit is larger than 10, we can use the pole zero plot represented in Fig.2- 24 to evaluate the impedance of the parallel RLC circuit. We obtain:

$$|Z(jn\omega_0)| = \frac{1}{C}\frac{l_{z0}}{l_{p1}l_{p2}} \approx \frac{n\omega_0}{C(n-1)\omega_0(n+1)\omega_0} = \frac{n}{C\omega_0(n^2-1)}$$

and $\arg[Z(jn\omega_0)] \approx -\frac{\pi}{2}$ for $n > 1$

along with $Z(j\omega_0) = R$. So:

$$v(t) \approx RI_1 \cos\omega_0 t + \sum_{n=2}^{\infty} \frac{nI_n}{C\omega_0(n^2-1)} \cos\left(n\omega_0 t - \frac{\pi}{2}\right)$$

$$= RI_1 \cos\omega_0 t + \sum_{n=2}^{\infty} \frac{nI_n}{C\omega_0(n^2-1)} \sin n\omega_0 t$$

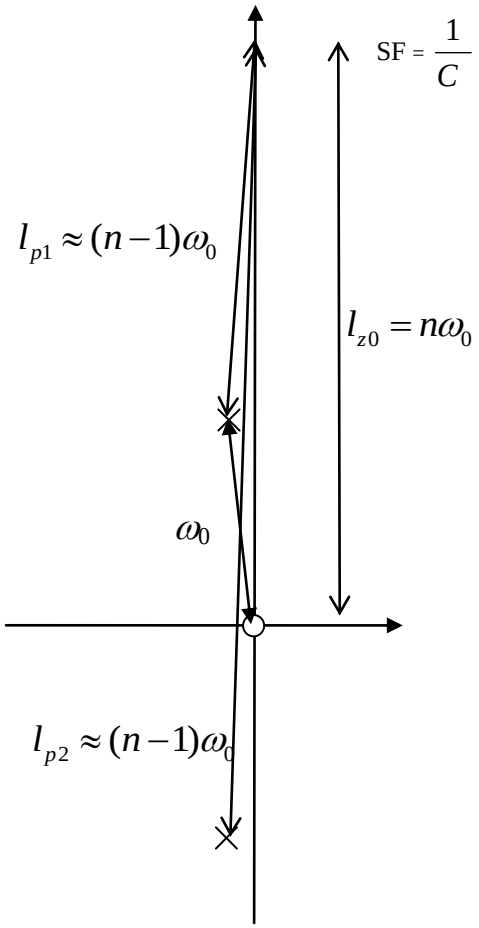


Fig.2- 24 pole zero plot for the harmonics

The above relation allows us to evaluate the distortion of the waveform before and after filtering.

Before filtering, the distortion coefficient is:

$$D_{before} = \sqrt{\sum_{n=2}^{\infty} \frac{I_n^2}{I_1^2}} \times 100\%$$

And after filtering, we have:

$$D_{after} = \sqrt{\sum_{n=2}^{\infty} \left[\frac{n}{RC\omega_0 (n^2 - 1)} \right]^2 \frac{I_n^2}{I_1^2}} \times 100\%$$

Chapter 3

Non Linear Controlled Sources

Communication circuits are built using passive matching networks and active devices. Most active devices act as voltage control current sources (BJT in Common Emitter or in Common Base, FET in Common Source or in Common Gate, etc). If the input voltage exceeds few millivolts, their transfer becomes highly nonlinear. In this chapter, we assume that the nonlinearity is memoriless. This simplifies the analysis of the different elements but it restricts the frequency range (in general, we cannot exceed the VHF band).

When we analyze nonlinear circuits, we cannot make use of the superposition theorem. This means that an analysis made for one type of waveform cannot be generalized to a linear combination of these waveforms. In our analysis of nonlinear controlled sources, we are going to restrict our analysis to systems excited by sinewaves or square waves. The output signal will be periodic with the same fundamental frequency as the input signal. Furthermore, since the nonlinear element is assumed memoriless, then, if the input is a sum of cosines (even function), the output will have the same parity and will also be a sum of cosines. The extreme waveforms that we will consider are the periodic train of impulses and the square wave.

The periodic train of impulses is useful in modeling very narrow current pulses.

Consider the current $i(t) = q\sum_{n=0}^{+\infty}\delta\left(t - nT_0\right)$. We have already encountered such signal in a previous course. It is periodic (period T_0) and can be developed in Fourier series. The coefficients of the series are all equal and the Fourier series is:

$$i(t) = \sum_{n=-\infty}^{+\infty}\frac{q}{T_0}e^{jn\omega_0 t} = \frac{q}{T_0}\left[1 + \sum_{n=1}^{+\infty}\left(e^{jn\omega_0 t} + e^{-jn\omega_0 t}\right)\right] = I_{dc}\left[1 + 2\sum_{n=1}^{+\infty}\cos n\omega_0 t\right] \qquad (7)$$

We remark that the fundamental and the harmonics have a peak amplitude equal to twice the dc current.

The other extreme case is the current that switches between a peak value I_p and zero with a period T_0 (square wave).

$$i(t)=\begin{cases} I_p & -\dfrac{T_0}{4}\le t\le \dfrac{T_0}{4} \\ 0 & \text{in the remaining part of the period} \end{cases}$$

In this case, the Fourier series is:

$$i(t)=\frac{I_p}{2}+\frac{2I_p}{\pi}\cos\omega_0 t-\frac{2I_p}{3\pi}\cos 3\omega_0 t+\frac{2I_p}{5\pi}\cos 5\omega_0 t-\cdots \qquad (8)$$

3.1 Piecewise linear characteristic

The first nonlinear source that we will consider is the piecewise linear one. It provides an adequate model for many MOSFET power amplifiers. This model is also encountered when we consider the effect of series resistance in many nonlinear amplifiers. Let us consider the following voltage controlled current source.

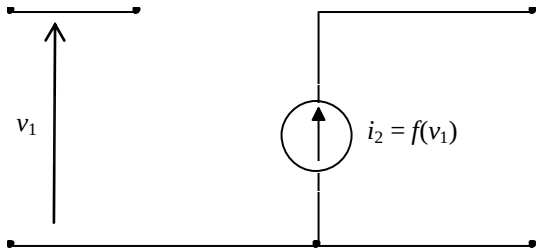


Fig.3- 1 Voltage Controlled Current Source

The transfer characteristic of the above controlled source is:

$$i_2=\begin{cases} G(v_1-V_0) & v_1\ge V_0 \\ 0 & v_1<V_0 \end{cases}$$

Graphically, this relation is represented by:

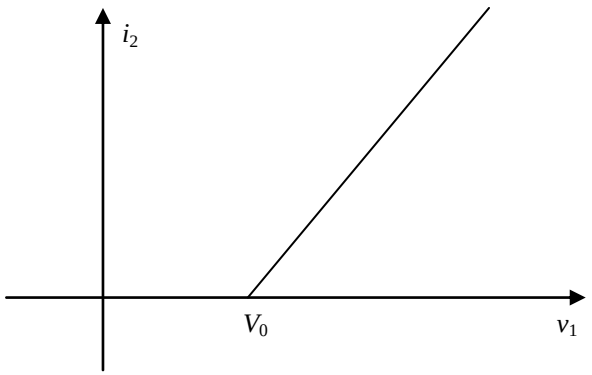


Fig.3- 2 Piecewise Linear Characteristic

The voltage V_0 is a threshold voltage. The slope G of the transfer function is a transconductance. The input signal is a sum of a biasing voltage V_b and an ac

signal $v(t)$: $v_1(t) = V_b + v(t)$. If the whole signal has a value larger than the threshold voltage, the transfer is incrementally linear. This means that the output current is expressed as:

$i_2(t) = I_b + i(t)$ along with $I_b = G(V_b - V_0)$ and $i(t) = Gv(t)$.

We remark that the ac signals are linearly related. However, we do not have the same relation between the dc signals. When the whole ac signal is amplified, we say that the amplifier is operating in "*class A*".

Another simple analytic case occurs when the biasing voltage V_b is equal to the threshold voltage V_0. This corresponds to "*class B*" operation. In this case, only the positive half of the ac signal is amplified and the operation is completely nonlinear. This implies that we cannot use an arbitrary ac voltage as input. Let us assume that this signal is sinusoidal: $v(t) = V_1 \cos \omega_0 t$. The output current is a half rectified sinewave as shown below.

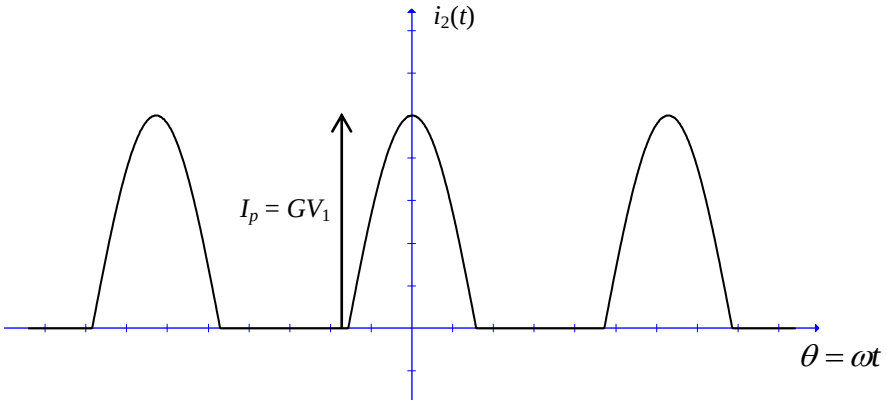


Fig.3- 3 Class B Output

We can develop the above signal in Fourier series. The result is:

$$i_2(t) = \frac{I_p}{\pi} + \frac{I_p}{2}\cos \omega_0 t + \frac{2I_p}{3\pi}\cos 2\omega_0 t - \frac{2I_p}{15\pi}\cos 4\omega_0 t + \cdots$$

and $I_p = GV_1$.

We remark that the dc output current is $\frac{GV_1}{\pi}$. Its value depends on the amplitude of the input signal. This means that if the device is biased using a current source, we must adjust the value of the biasing current every time the input voltage changes in order to maintain the biasing voltage at the value $V_b = V_0$.

Another point worth taking into account is that the peak value of the fundamental current is proportional to the input voltage. If we load the output circuit with a parallel RLC circuit tuned at the fundamental and with a Q high enough so that the harmonics are practically eliminated, the output voltage will

be: $v_0(t) = \frac{RI_p}{2}\cos\omega_0 t = \frac{RG}{2}V_1\cos\omega_0 t = \frac{RG}{2}v(t)$. This means that the output voltage is proportional to the input one. The amplitude of the output is proportional to the amplitude of the input. Thus, an amplifier biased in class B can be used to amplify "*linearly*" an amplitude modulated signal. The device amplifies half of the waveform and the tank circuit recovers the other half. If the signal is modulated (AM, VSB, SSB, QAM), we must make sure that the bandwidth of the parallel RLC circuit is wide enough to let the modulation pass without affecting it adversely.

If now the biasing voltage V_b is different from the threshold voltage V_0, but the ac signal does not pass completely, we have to define a "*conduction angle*". In this case also, we study the case of a sinewave drive $v(t) = V_1\cos\omega_0 t$.

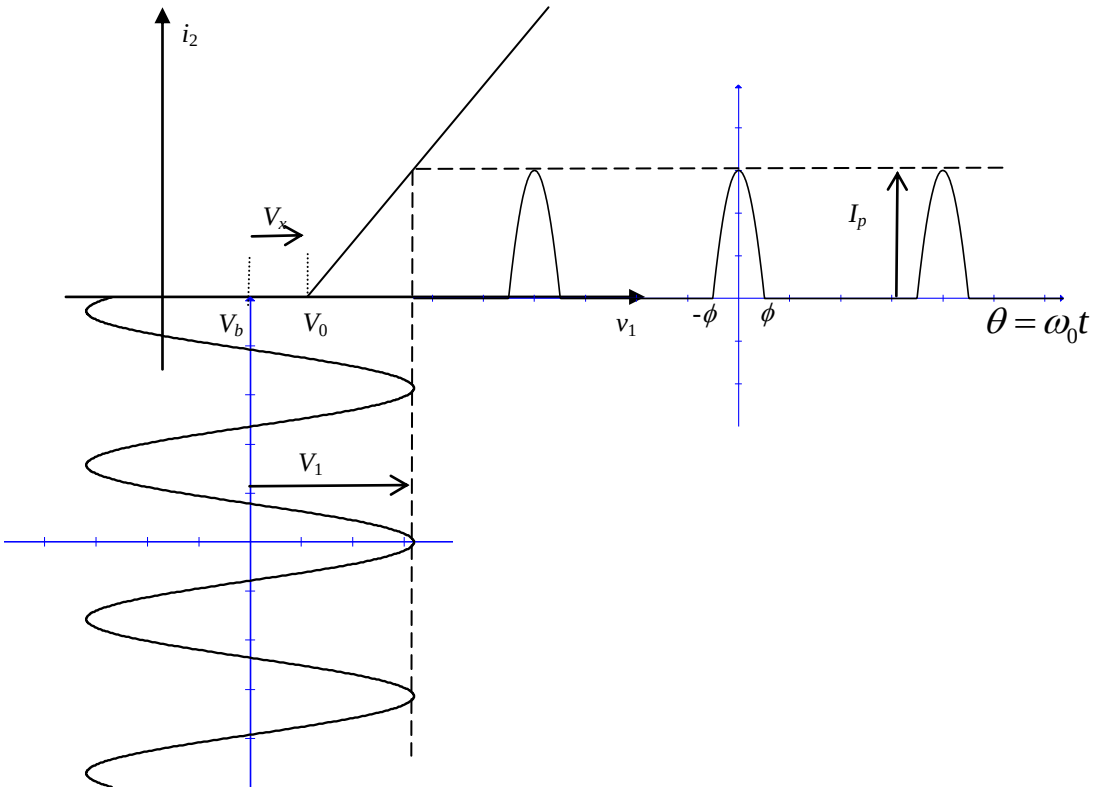


Fig.3- 4 Class C Biasing

In the above figure, we define $V_x = V_b - V_0$ and $I_p = G(V_1 - V_x)$. Using the variable $\theta = \omega_0 t$, we remark that the controlled source produces an output current for $-\phi \le \theta \le \phi$, i.e. for a "*conduction angle*" equal to 2ϕ. The angle ϕ is given by:

$$\phi = \cos^{-1}\left(\frac{V_x}{V_1}\right)$$

Using the above definition of a conduction angle (2ϕ), we can give now a precise definition of the different classes of amplification:

- Class A: Conduction angle = 2ϕ = 360°. The whole sinewave passes through the system.
- Class B: Conduction angle = 180°. Only the positive half of the sinewave is amplified.
- Class AB: Conduction angle is such that $180° < 2\phi < 360°$.
- Class C: Conduction angle is such that $0 < 2\phi < 180°$. Only a small tip of the sinewave is amplified.

If we consider the voltage V_x, the class C corresponds to $V_x > 0$, i.e. $V_b < V_0$ while class AB corresponds to $V_x < 0$, i.e. $V_b > V_0$. The output current is not sinusoidal and can be developed in Fourier series.

The system is memoriless and since the input is an even function, the output current is also even and its Fourier series is then a sum of cosine functions.

$$i_2(t) = \sum_{n=0}^{+\infty} I_n \cos n\omega_0 t$$

The computation of the Fourier coefficients is simplified if we use the variable $\theta = \omega_0 t$. We have:

$$I_0 = \frac{1}{\pi}\int_0^{\phi} i_2\left(\frac{\theta}{\omega_0}\right) d\theta \text{ and } I_n = \frac{2}{\pi}\int_0^{\phi} i_2\left(\frac{\theta}{\omega_0}\right)\cos n\theta d\theta$$

The expression of the output current in the interval $[-\phi,\phi]$ is just a shifted sinewave:

$i_2(t) = G(V_1\cos\omega_0 t - V_x)$ for $-\phi \le \theta = \omega_0 t \le \phi$. So:

$$i_2\left(\frac{\theta}{\omega_0}\right) = G(V_1\cos\theta - V_x)$$

Replacing in the expression of the Fourier coefficients, we obtain[2]:

$$I_0 = \frac{I_p}{\pi}\frac{\sin\phi - \phi\cos\phi}{1-\cos\phi}$$

$$I_1 = \frac{I_p}{\pi}\frac{\phi - \cos\phi\sin\phi}{1-\cos\phi}$$

$$I_n = \frac{2I_p}{\pi}\frac{\cos\phi\sin n\phi - n\sin\phi\cos n\phi}{n\left(n^2-1\right)(1-\cos\phi)} \qquad n \ge 2$$

These currents are given below (Fig.3- 5) as a function of the conduction angle (2ϕ). The next figure (Fig.3- 6) provides the same information, but with the

[2] See Appendix to Chapter 4 of textbook for details.

normalized voltage offset $\left(\frac{V_x}{V_1}\right)$ as argument. They are also plotted in your textbook in pp.94-95, Fig.4.2-3 and Fig.4.2-4 but with a logarithmic scale.

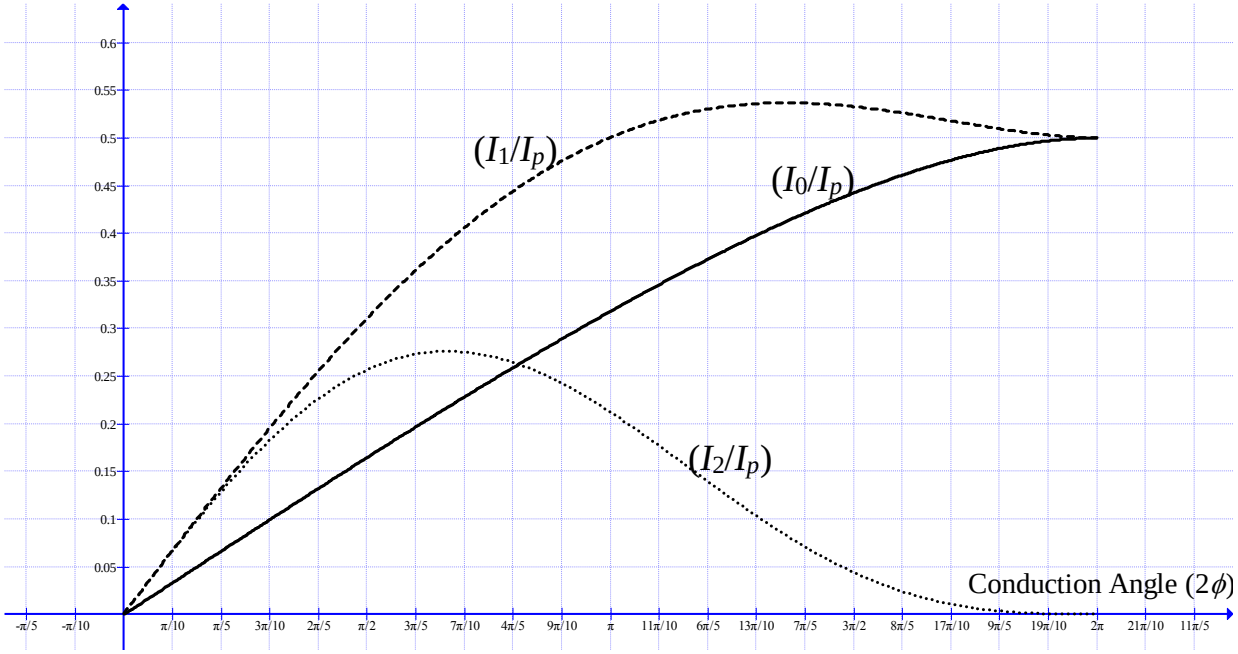


Fig.3- 5 DC, Fundamental and Second Harmonic for Sine Tips

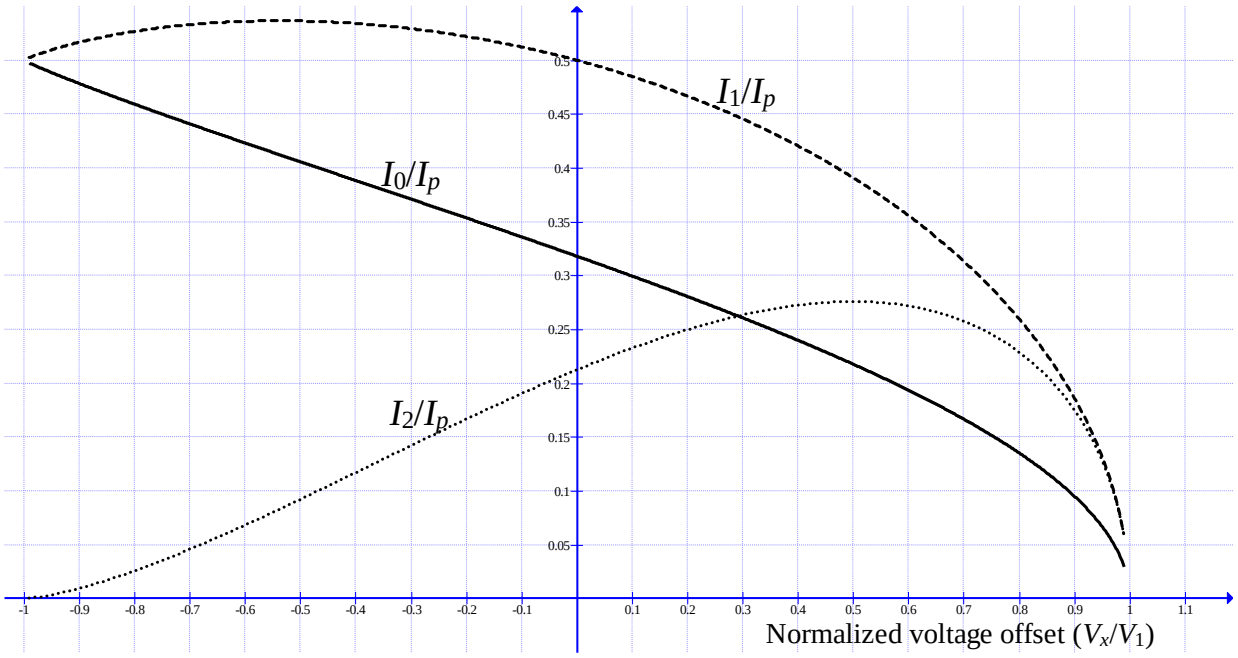


Fig.3- 6 DC, Fundamental and Second Harmonic vs Normalized Voltage Offset

If we use Taylor approximations for the coefficients I_n, we can remark that $\lim_{\phi \to 0} \frac{I_n}{I_0} = 2$ for $n \geq 1$. This means that the current approaches an impulse train as the conduction angle becomes small. We will see that many amplifiers have this behavior when the input amplitude becomes large.

3.2 Square law characteristic

Another characteristic commonly used in communication circuits is the transfer characteristic of the FET devices. The transfer that we will study is the one of the N channel JFET. The obtained results can easily be extended to MOSFET transistors. By reversing polarities, the same results are valid for P channels of both types.

The square law characteristic is given by:

$$i_2 = I_{DSS}\left(1 - \frac{v_1}{V_p}\right)^2 \qquad ; \qquad V_p \leq v_1 \leq 0$$

$$= 0 \qquad ; \qquad v_1 < V_p$$

The region corresponding to positive values of input voltages is a forbidden region.

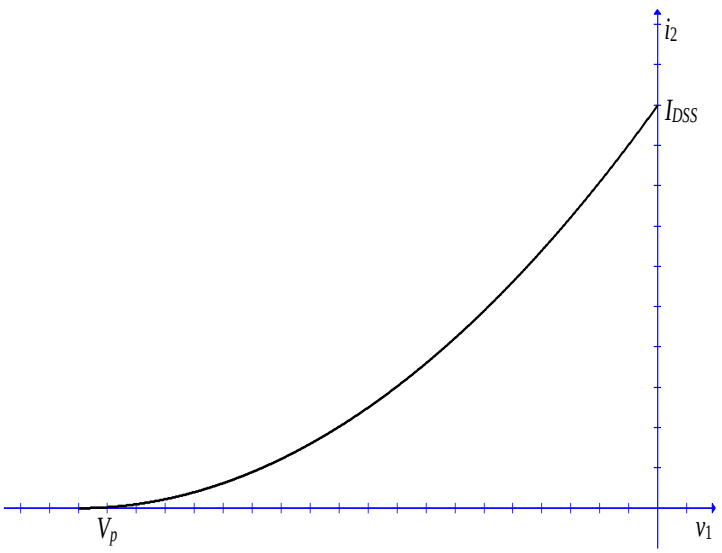


Fig.3- 7 Square law Characteristic

As usual, we assume that the input signal is a dc biasing voltage added to an ac signal. $v_1(t) = V_b + v(t)$. The first case we will analyze is the one of a very small input ac voltage ($|v(t)| << 1$). We use Taylor's approximation and we obtain:

$i_2(t) = I_b + i(t)$ where $i(t) = g_m v(t)$. g_m is the small signal transconductance at the Q point V_b, I_b. It is defined by:

$$g_m = \left.\frac{di_2}{dv_1}\right|_{v_1=V_b} = \left.\frac{-2I_{DSS}}{V_p^2}\left(V_p - v_1\right)\right|_{v_1=V_b}$$

The expression of the small signal transconductance is:

$$g_m = \frac{-2I_{DSS}}{V_p^2} V_x$$

$V_x = V_p - V_b$

For JFET, the small signal transconductance varies between 0 (for $V_b = V_p$) and a maximum value:

$g_{m0} = \dfrac{-2I_{DSS}}{V_p}$ obtained when $V_b = 0$.

The voltage gain is then maximum when the biasing voltage is zero (the biasing current is equal to I_{DSS}).

If the ac signal is large, we restrict the analysis to the sinewave case $v(t) = V_1 \cos\omega_0 t$. There are two possible cases: The ac signal is completely inside the square law region ($V_p \le V_b - V_1 \le V_b + V_1 \le 0$) or only the tip of the sinewave is amplified.

The first case is fairly simple. Starting from:

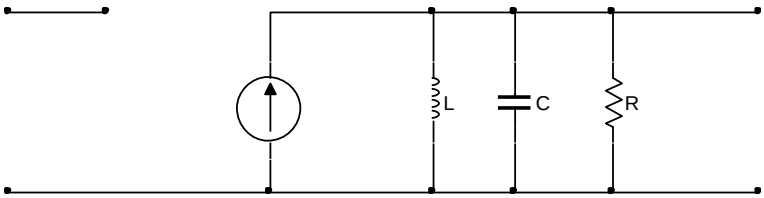
$$i_2 = I_{DSS}\left(1 - \frac{v_1}{V_p}\right)^2 = \frac{I_{DSS}}{V_p^2}\left(V_p - v_1\right)^2$$

and replacing $v_1 = V_b + V_1 \cos\omega_0 t$, we obtain the following Fourier series:

$$i_2 = I_0 + I_1 \cos\omega_0 t + I_2 \cos 2\omega_0 t$$

$$I_0 = \frac{I_{DSS}}{V_p^2}\left(V_x^2 + \frac{V_1^2}{2}\right);\ I_1 = -2\frac{I_{DSS}}{V_p^2} V_x V_1;\ I_2 = \frac{I_{DSS}}{V_p^2}\frac{V_1^2}{2}. \qquad V_x = V_p - V_b.$$

The Fourier series contains only three terms: dc, fundamental and second harmonic. If we load the output with a parallel RLC circuit tuned at the fundamental, the coefficient I_1 will be the only one that will produce an output.



For such system, we can define a "*large signal transconductance*" G_m as being the ratio of the peak amplitude of the fundamental of the output current over the peak amplitude of the input voltage.

$$G_m = \frac{I_1}{V_1}$$

And the output ac voltage is $v_0(t) = RG_m v(t) = G_m RV_1 \cos\omega_0 t$ (The dc and the second harmonic are eliminated by the tank circuit). The voltage gain is: $A = G_m R$. In our case, the large signal transconductance is given by:

$$G_m = -\frac{2I_{DSS}}{V_p^2} V_x$$

The expression of the large signal transconductance is identical to the small signal one. However, the large signal transconductance applies only to a sinewave drive along with a high Q parallel RLC as a load. The small signal transconductance, on the other hand, applies to the case of an arbitrary small input drive.

If now the signal has values outside the interval [V_p, 0], we will have more harmonics in the output current. This is due to the fact that only the tip of the sinewave is amplified. In this case also, we can define a conduction angle 2ϕ with $\phi = \cos^{-1}\left(\frac{V_x}{V_1}\right)$. The output current is also given as a function of this conduction angle.

$$i_2(t) = \sum_{n=0}^{+\infty} I_n \cos n\omega_0 t$$

with a peak output value $I_p = \left(\frac{I_{DSS}}{V_p^2}\right)(V_1 - V_x)^2$.

The coefficients are plotted in your textbook pp. 102-103, Fig.4.4-4 and Fig.4.4-5. The analytic formulation is provided in the appendix of chapter 4, p.147.

3.3 Exponential characteristic

This transfer characteristic is a good model of a bipolar junction transistor driven by an ideal voltage source. In order to apply it to actual circuits, we must make sure that the transistor is operating in normal mode. One particularity of this transfer characteristic is the absence of a threshold. The output current is related to the input voltage by

$$i_2 = I_s \exp\left(\frac{qv_1}{kT}\right)$$

We have already seen that kT/q is approximately 26 mV at 300°K.

The input voltage is $v_1 = V_b + v(t)$ as in the previous sections. The small signal transfer is obtained when $|v(t)| << 1$. At that time, we can use a first order approximation for the exponential $e^z \approx 1 + z$. We obtain:

$$i_2 = I_s \exp\left(\frac{qV_b}{kT}\right)\exp\left(\frac{qv(t)}{kT}\right) \approx I_s \exp\left(\frac{qV_b}{kT}\right)\left(1 + \frac{qv(t)}{kT}\right)$$

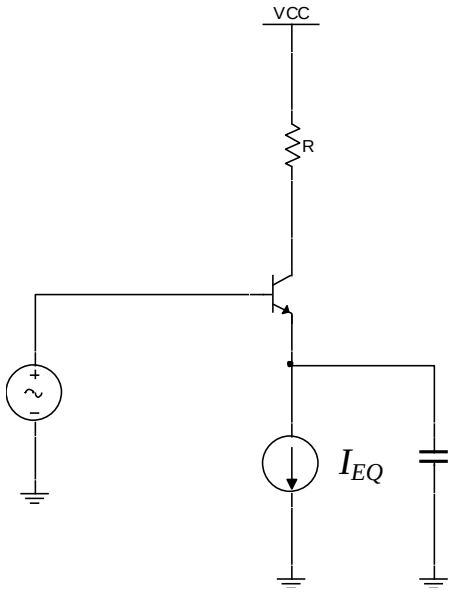
The output current is equal to a dc current added to an ac current:

$i_2 = I_{dc} + i(t)$ where $I_{dc} = I_s \exp\left(\frac{qV_b}{kT}\right)$ and $i(t) = \frac{qI_{dc}}{kT} v(t)$.

The ac signals are linearly related by the following small signal transconductance:

$$g_m = \frac{qI_{dc}}{kT}$$

For example, if we consider an NPN transistor biased by a current source I_{EQ}



The voltage at the collector is given by:

$v_c(t) = \text{Vcc} - Ri_C(t) = \text{Vcc} - \alpha RI_{EQ} - g_m Rv(t)$ where $g_m = \alpha \frac{qI_{EQ}}{kT}$ when the input is less than few millivolts (as in Lab #1).

If the amplitude of the input becomes larger, we cannot use the above approximation and the system is highly nonlinear. We consider the sinewave case only. So, let the input be:

$v_1 = V_b + v(t)$ where $v(t) = V_1 \cos \omega_0 t$.

The current is then: $i_2 = I_s \exp\left(\frac{qV_b}{kT}\right)\exp\left(\frac{qV_1}{kT}\cos\omega_0 t\right)$.

Let $x = \frac{qV_1}{kT}$ be the input amplitude normalized to 26 mV. The current is:

$i_2 = I_s \exp\left(\frac{qV_b}{kT}\right)\exp\left(x\cos\omega_0 t\right)$. This current has values that vary between a peak value I_p when $\cos\omega_0 t$ = +1 and a minimum value I_m when $\cos\omega_0 t$ = –1. The peak value is:

$$I_p = I_s \exp\left(\frac{qV_b}{kT}\right)e^x$$

If we normalize i_2 to I_p, we obtain the following:

$$W_x(t) = \frac{i_2}{I_p} = \frac{e^{x\cos\omega_0 t}}{e^x}$$

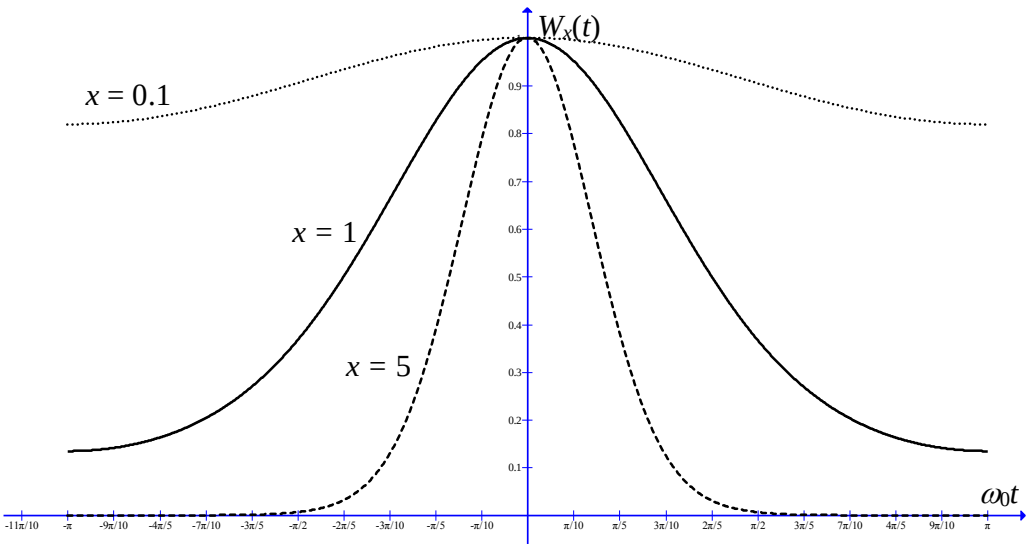


Fig.3- 8 Normalized current

This normalized current is plotted above for different values of x. We see that when x is small, the current is practically sinusoidal. This character disappears for larger values. You can observe this behavior in lab#1. The following figure is a display of the output of part 2 of lab#1 for an input of 26 mV, i.e. x = 1.

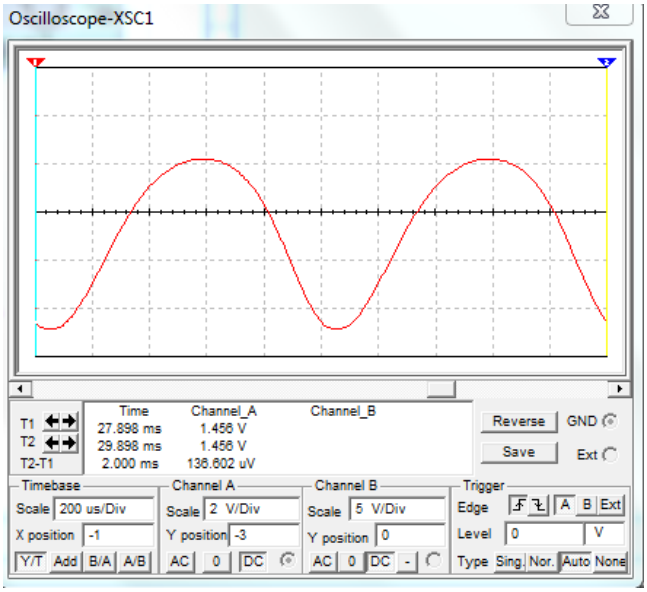


Fig.3- 9 Lab#2 Scope display for $x = 1$

We can remark the typical distortion of the exponential characteristic. The figure is reversed with respect to Fig.3- 8 because we are displaying the voltage at the collector of the transistor: $v_C(t) = \mathrm{Vcc} - \mathrm{Rc}i_2(t) = \mathrm{Vcc} - \mathrm{Rc}W_x(t)I_p$.

Now, the function $\exp(x\cos\omega_0 t)$ is periodic and it can be developed in Fourier series. We have seen in chapter 1 that:

$$\exp(x\cos\omega_0 t) = I_0(x) + 2\sum_{n=1}^{\infty} I_n(x)\cos n\omega_0 t$$

where the functions $I_n(x)$ are the modified Bessel functions of the first kind. These functions are tabulated in your textbook. Using the above relation, we can write:

$$i_2(t) = I_s \exp\left(\frac{qV_b}{kT}\right) I_0(x)\left[1 + \sum_{n=1}^{\infty} \frac{2I_n(x)}{I_0(x)}\cos n\omega_0 t\right]$$

or

$$i_2(t) = I_{dc}\left[1 + \sum_{n=1}^{\infty} \frac{2I_n(x)}{I_0(x)}\cos n\omega_0 t\right]$$

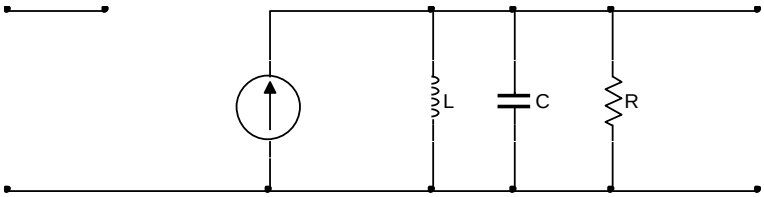
I_{dc} is the dc current flowing in the output branch of the circuit. If the circuit is biased using a current source, its value is fixed and does not depend on the input voltage. However, if the circuit uses resistive biasing, its value will depend on that voltage. We also remark that the fundamental and the harmonics are given by $I_{dc}\dfrac{2I_n(x)}{I_0(x)}$. This ratio of modified Bessel functions is provided in the next table (following page) taken from your textbook.

x	$2I_1(x)/I_0(x)$	$2I_2(x)/I_0(x)$	$2I_3(x)/I_0(x)$	$2I_4(x)/I_0(x)$	$2I_5(x)/I_0(x)$
0.0	0.0	0.0	0.0	0.0	0.0
0.5	0.4850	0.0600	0.0050	0.0003	0.0000
1.0	0.8928	0.2144	0.0350	0.0043	0.0004
1.5	1.1923	0.4103	0.0981	0.0179	0.0026
2.0	1.3955	0.6045	0.1866	0.0445	0.0086
2.5	1.5300	0.7760	0.2884	0.0839	0.0200
3.0	1.6200	0.9200	0.3933	0.1335	0.0374
3.5	1.6822	1.0387	0.4951	0.1900	0.0607
4.0	1.7270	1.1365	0.5906	0.2506	0.0893
4.5	1.7607	1.2175	0.6785	0.3129	0.1222
5.0	1. 768	1.2853	0.7585	0.3751	0.1584
5.5	1.8076	1.3427	0.8311	0.4360	0.1970
6.0	1.8247	1.3918	0.8969	0.4949	0.2370
6.5	1.8390	1.4342	0.9564	0.5513	0.2779
7.0	1.8511	1.4711	1.0104	0.6050	0.3189
7.5	1.8615	1.5036	1.0595	0.6560	0.3598
8.0	1.8705	1.5324	1.1043	0.7042	0.4001
8.5	1.8784	1.5580	1.1452	0.7497	0.4396
9.0	1.8854	1.5810	1.1827	0.7926	0.4782
9.5	1.8916	1.6018	1.2172	0.8330	0.5157
10.0	1.8972	1.6206	1.2490	0.8712	0.5520
10.5	1.9022	1.6377	1.2784	0.9072	0.5872
11.0	1.9068	1.6533	1.3056	0.9412	0.6211
11.5	1.9110	1.6677	1.3309	0.9733	0.6538
12.0	1.9148	1.6809	1.3545	1.0036	0.6854
12.5	1.9183	1.6931	1.3765	1.0324	0.7157
13.0	1.9215	1.7044	1.3970	1.0596	0.7450
13.5	1.9244	1.7149	1.4163	1.0854	0.7731
14.0	1.9272	1.7247	1.4344	1.1099	0.8002
14.5	1.9298	1.7338	1.4515	1.1332	0.8262
15.0	1.9321	1.7424	1.4675	1.1554	0.8513
15.5	1.9344	1.7504	1.4827	1.1765	0.8754
16.0	1.9365	1.7579	1.4970	1.1966	0.8987
16.5	1.9384	1.7650	1.5105	1.2158	0.9211
17.0	1.9403	1.7717	1.5234	1.2341	0.9426
17.5	1.9420	1.7781	1.5356	1.2516	0.9634
18.0	1.9436	1.7840	1.5472	1.2683	0.9835
18.5	1.9452	1.7897	1.5582	1.2843	1.0028
19.0	1.9466	1.7951	1.5687	1.2997	1.0215
19.5	1.9480	1.8002	1.5788	1.3144	1.0395
20.0	1.9493	1.8051	1.5883	1.3286	1.0569

Fig.3- 10 Normalized current harmonics

One particularity of the modified Bessel function is that $\lim_{x\to\infty}\frac{2I_n(x)}{I_0(x)}=2$. This means that for large *x*, the Fourier development of the current becomes the one of a periodic impulse train. Another point worth noting is that it is very hard to define a *conduction angle*. In fact, the current is never zero. In your textbook, the conduction angle is defined for a current equal to 5% of the peak value.

If the amplifier is loaded with a high Q tank circuit tuned at the fundamental, the output voltage will be sinusoidal.



As we did with the square law characteristic, we can define here also a large signal transconductance:

$$G_m(x)=\frac{I_{dc}\dfrac{2I_1(x)}{I_0(x)}}{V_1}=\frac{qI_{dc}}{kT}\frac{2I_1(x)}{xI_0(x)}=g_m\frac{2I_1(x)}{xI_0(x)}$$

Giving a normalized value of:

$$\frac{G_m(x)}{g_m}=\frac{2I_1(x)}{xI_0(x)}$$

This function is tabulated below.

x	$\frac{2I_1(x)}{xI_0(x)}=\frac{G_m(x)}{g_m}$
0.0	1.0
0.2	0.995
0.5	0.970
1.0	0.893
2.0	0.698
3.0	0.540
4.0	0.432
5.0	0.357
6.0	0.304
7.0	0.264
8.0	0.234
9.0	0.210
10.0	0.190
15.0	0.129
20.0	0.0975

This function is plotted below.

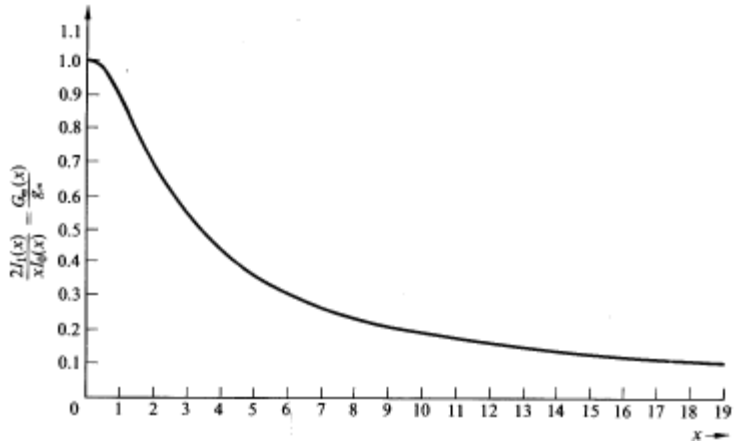


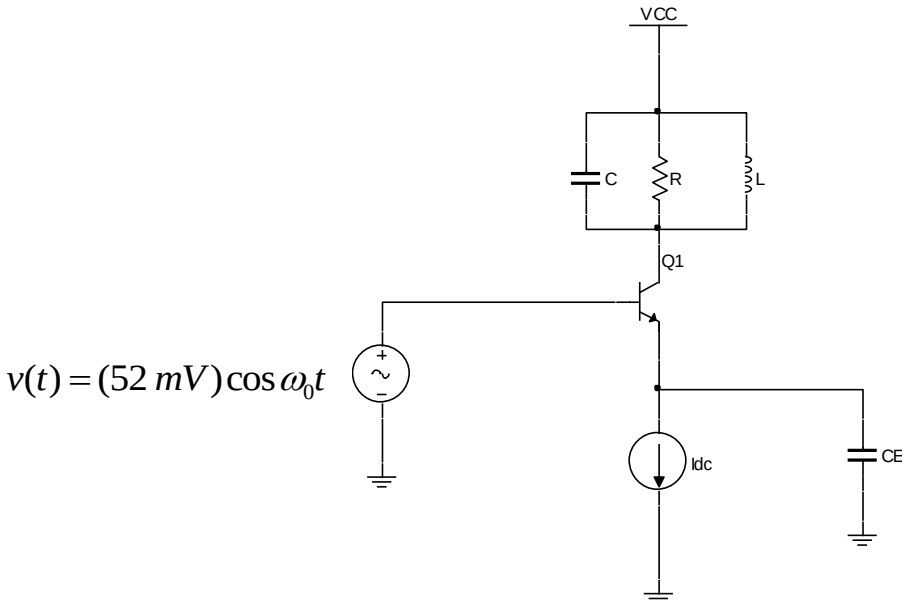
Fig.3- 11 Normalized large signal transconductance

We can use this large signal transconductance to express the output voltage across the tank circuit:

$$v_o(t) = G_m R V_1 \cos\omega_0 t$$

We can remark that the gain decreases with increasing values of the input. This behavior can be used to stabilize the amplitude of many systems such as the sinusoidal oscillators. This decrease of gain can be explained by the fact that, as the amplitude increases, most of the power is distributed to the harmonics rather than to the fundamental. So, even though the output amplitude is increasing as x is increasing, its ratio with the input is decreasing.

Example:



$v(t) = (52\,mV)\cos\omega_0 t$

Let us consider the above circuit. The tank circuit is tuned at ω_0 and the resistance R has the value of 1 kΩ. The power supply voltage VCC has the value of 10 V. The current Idc has the value of 1 mA. We have: $x = \frac{52}{26} = 2$, giving a

fundamental current $I_1 = 1.3955 \times (1\,\text{mA})$. The voltage at the collector of the transistor is equal to

$$v_C(t) = \text{VCC} - RI_1 \cos\omega_0 t = 10\text{V} - (1\,\text{k}\Omega \times 1.3955\ \text{mA})\cos\omega_0 t = 10\ \text{V} - (1.3955\ \text{V})\cos\omega_0 t$$

We can find the same result using transconductance calculation. The small signal transconductance is: $g_m = \dfrac{1\,\text{mA}}{26\,\text{mV}} = 0.0385\,\Omega^{-1}$. For $x = 2$, we have $\dfrac{G_m(2)}{g_m} = 0.698$ giving $G_m(2) = 0.0268\,\Omega^{-1}$. This gives:

$$v_C(t) = \text{VCC} - G_m(x)RV_1 \cos\omega_0 t$$
$$v_C(t) = 10\,\text{V} - 0.0268 \times 1000 \times 52 \times 10^{-3} \cos\omega_0 t$$
$$v_C(t) = 10\ \text{V} - (1.3936\ \text{V})\cos\omega_0 t$$

We obtain practically the same result using both methods. The differences in the results are mainly due to rounding errors.

If we want to increase the output without increasing the distortion, we can increase the biasing current (this will increase the value of the small signal transconductance) or we can increase the value of the load resistance (in this case we are limited by the value of the finite output resistance).

3.4 Resistively biased BJT

When the biasing current is fixed by a current source, we have seen that the analysis of a BJT amplifier is straightforward. The dc current is given. However, if we use resistors to produce the biasing, the voltage across these resistors is stored in capacitors and this voltage will depend on the applied ac voltage.

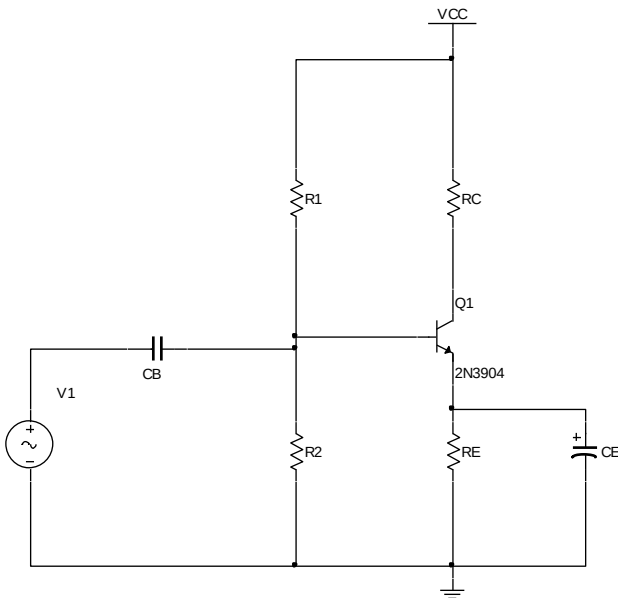


Fig.3- 12 Resistively biased BJT

The above figure shows a resistively biased BJT. By using Thevenin theorem, we can transform the base circuit as follows:

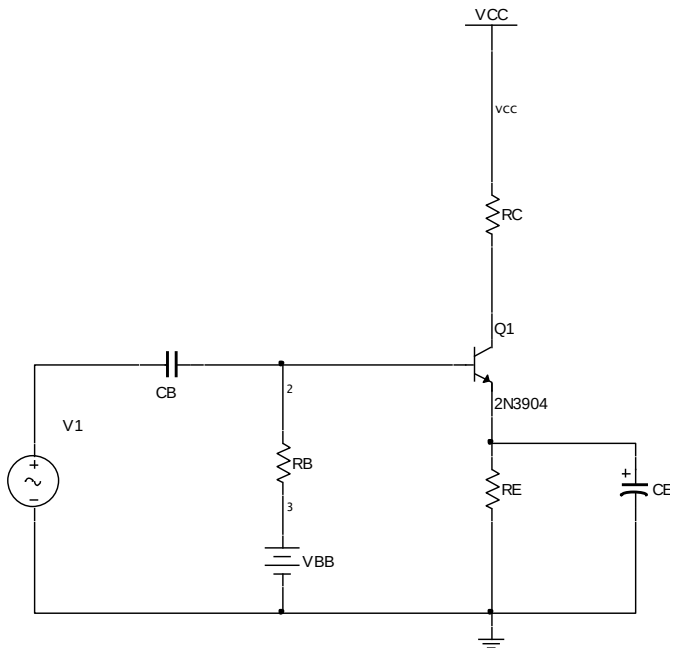


Fig.3- 13 Base equivalent circuit

where $R_B = \dfrac{R_1 R_2}{R_1 + R_2}$ and $V_{BB} = V_{CC} \dfrac{R_2}{R_1 + R_2}$.

The above circuit is shown with a resistive load; however, the load R_C can be replaced by a parallel tank circuit. In the analysis of the circuit, we assume that the transistor is operating in the normal mode. So, the emitter current is related with the base emitter voltage by the usual exponential characteristic:

$$i_E = I_{ES} \exp\left(\frac{q v_{BE}}{kT} \right)$$

and $i_C = \alpha i_E$ along with $i_B = (1-\alpha) i_E = \dfrac{i_E}{\beta + 1}$.

If the base emitter voltage is only a dc one (no signal), the dc current flowing through the emitter is given by:

$$I_{EQ} = \frac{V_{BB} - V_{dcQ}}{R_E + (1-\alpha) R_B} \tag{9}$$

The voltage $V_{dcQ} = v_{BEQ}$ is the dc voltage that appears across the series connection of the two capacitors C_B and C_E (the ac voltage source at the input is shorted to ground). Its value is also related to the current flowing in the transistor by:

$$V_{dcQ} = \frac{kT}{q} \ln \frac{I_{EQ}}{I_{ES}} \tag{10}$$

For a discrete transistor biased with a current between 0.1 to 10 mA, the value of V_{dcQ} remains around 650 mV. If we want to compute its value, we can use the iterative method shown in chapter 1.

Now, if we apply an ac voltage at the input ($v(t) = V_1 \cos \omega_0 t$), the value of the dc voltage changes from V_{dcQ} to V_{dc} and this will entail a change in the dc current from I_{EQ} to I_{E0}. The new equations are now:

$$v_{BE}(t) = V_{dc} + V_1 \cos \omega_0 t$$

giving

$$i_E(t) = I_{ES} \exp\left(\frac{qV_{dc}}{kT} \right) \exp\left(\frac{qV_1}{kT} \cos \omega_0 t \right) = I_{ES} \exp\left(\frac{qV_{dc}}{kT} \right) \exp\left(x \cos \omega_0 t \right)$$

Using the Fourier series development seen in the previous section, we obtain:

$$i_E(t) = I_{ES} \exp\left(\frac{qV_{dc}}{kT} \right) I_0(x) \left[1 + \sum_{n=1}^{\infty} \frac{2I_n(x)}{I_0(x)} \cos n\omega_0 t \right]$$

or $i_E(t) = I_{E0} \left[1 + \sum_{n=1}^{\infty} \frac{2I_n(x)}{I_0(x)} \cos n\omega_0 t \right]$

We can now rewrite equations (9) and (10) for a sinewave input as:

$$I_{E0} = \frac{V_{BB} - V_{dc}}{R_E + (1-\alpha) R_B} \tag{11}$$

and

$$I_{E0} = I_{ES} \exp\left(\frac{qV_{dc}}{kT} \right) I_0(x) \tag{12}$$

Since V_{dc} is different from V_{dcQ}, let us write:

$$V_{dc} = V_{dcQ} - \Delta V$$

If we replace in (11), we obtain:

$$I_{E0} = \frac{V_{BB} - V_{dcQ}}{R_E + (1-\alpha) R_B} + \frac{\Delta V}{R_E + (1-\alpha) R_B}$$

$$I_{E0} = I_{EQ} + \frac{\Delta V}{R_E + (1-\alpha) R_B} = I_{EQ} \left[1 + \frac{\Delta V}{V_\lambda} \right] \tag{13}$$

where $V_\lambda = \left(R_E + (1-\alpha) R_B \right) I_{EQ}$.

Equation (12) on the other hand produces:

$$I_{E0} = I_{EQ} \exp\left(-\frac{q\Delta V}{kT} \right) I_0(x) \tag{14}$$

Equating (13) and (14), we obtain:

$$\left[1+\frac{\Delta V}{V_\lambda}\right]=\exp\left(-\frac{q\Delta V}{kT}\right)I_0(x)$$

The above equation does not have an analytic solution. However, it is shown in the textbook, that, if V_λ is larger than 520 mV, we can safely neglect the term $\frac{\Delta V}{V_\lambda}$ in the above equation. We finally get:

$$\Delta V=\frac{kT}{q}\ln I_0(x)$$

Now, we can express the relationship that exists between the two dc currents:

$$I_{E0}=I_{EQ}\left[1+\frac{\ln I_0(x)}{\left(\frac{qV_\lambda}{kT}\right)}\right]$$

So, if x is small and V_λ large, we can safely assume that the two currents are the same. However, if the design is not very good (small V_λ), the two currents will be quite different when the amplitude of the input signal increases.

If we want to neglect the effect of the input drive and have practically $I_{E0} = I_{EQ}$ within 5%, we must have:

$$20\ln I_0(x)<\left(\frac{qV_\lambda}{kT}\right)$$

This relation is shown in the next figure.

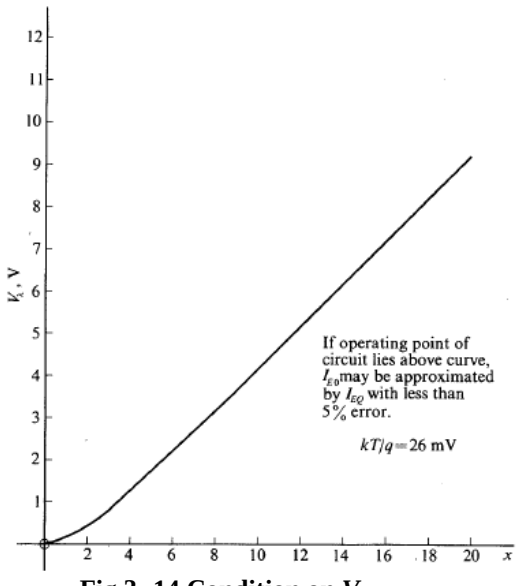


Fig.3- 14 Condition on V_λ

For example, if the input signal has a peak value of 260 mV, the voltage V_λ must be larger than 4 V.

3.5 Differential Characteristic

In our collection of nonlinearities, the differential characteristic is one of the most important. This circuit is commonly used in integrated circuits. We will see later that it is the basic building block of the double balanced mixer-modulator. We also find it in the implementation of IF amplifiers used in FM receivers. This is due to the fact that it is a very good amplitude limiter.

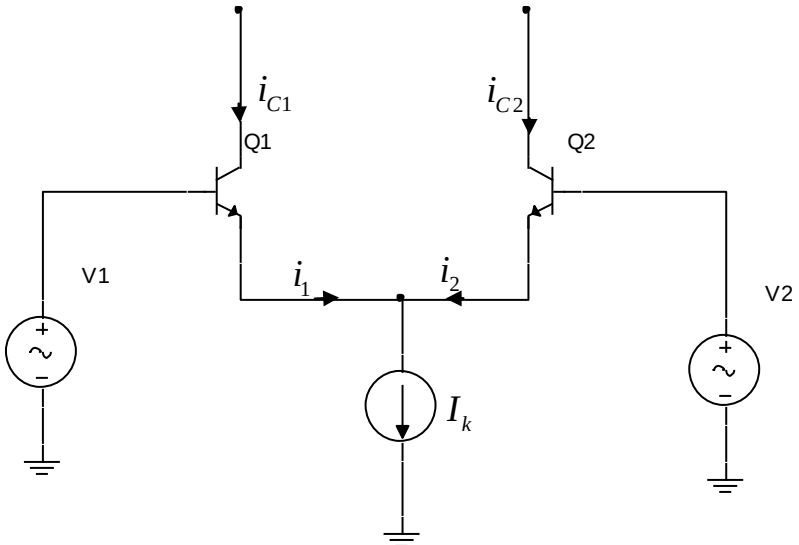


Fig.3- 15 Differential Amplifier

In the circuit of Fig.3- 15, the current I_k is divided between the two transistors. This means that any value of the input voltages, the current in each transistor will never exceed the value of I_k. The node equation at the emitter of the two transistors is:

$$i_1 + i_2 = I_k$$

This implies that the variations of the two currents are opposite. When one increases, the other one decreases by the same amount.

We assume that the two transistors are identical. The basic equations are:

$$i_1 = I_S \exp\left(\frac{qv_{BE1}}{kT}\right) \text{ and } i_2 = I_S \exp\left(\frac{qv_{BE2}}{kT}\right)$$

So: $\frac{i_1}{i_2} = \exp\left(\frac{q}{kT}\left(v_{BE1} - v_{BE2}\right)\right) = \exp\left(\frac{q}{kT}\left(v_1 - v_2\right)\right)$

Let us define: $z = \frac{q}{kT}\left(v_1 - v_2\right)$. The emitter currents become:

$$i_1 = \frac{I_k}{1+e^{-z}} \text{ and } i_2 = \frac{I_k}{1+e^{z}}$$

The above expressions do not show clearly the fact that when one current increases by a given amount, the other decreases by exactly the same value. The average value for both currents is $\frac{I_k}{2}$. Let i be a variation around this value.

$i_1 = \frac{I_k}{2} + i$ and $i_2 = \frac{I_k}{2} - i$. The variation of current is:

$i = \frac{I_k}{2}\tanh\left(\frac{z}{2}\right)$ and finally the two currents can be expressed as:

$i_1 = \frac{I_k}{2}\left[1+\tanh\left(\frac{z}{2}\right)\right]$ and $i_2 = \frac{I_k}{2}\left[1-\tanh\left(\frac{z}{2}\right)\right]$.

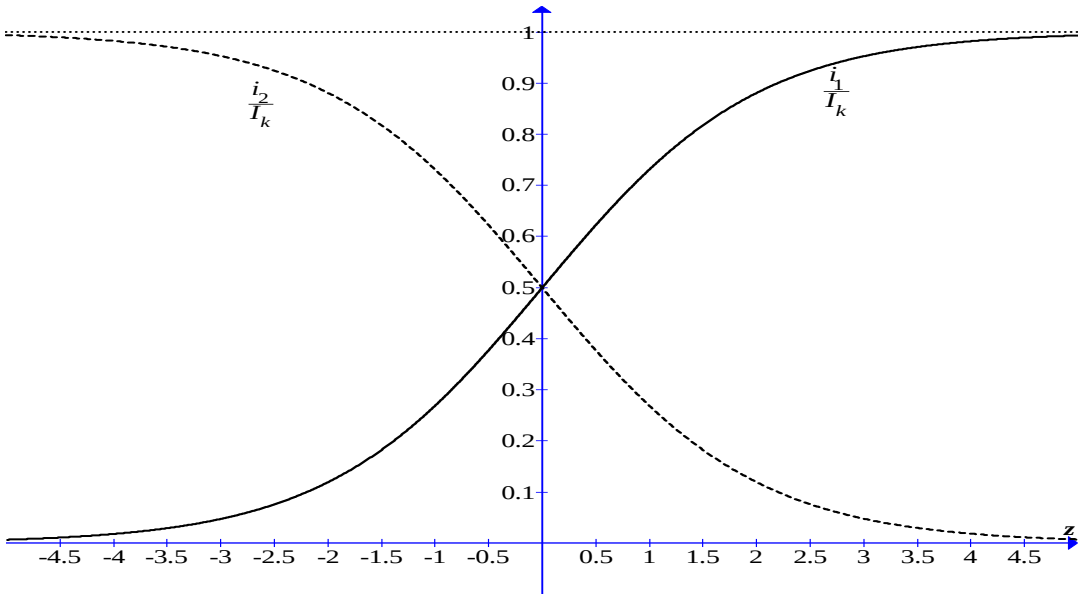


Fig.3- 16 Emitter currents

The above figure shows the variation of the two currents as a function of the normalized input. It shows clearly the opposite variation of the two currents. Another point worth noticing is the fact that when the input is sinusoidal with large amplitude, the output becomes practically a square wave.

If the input signal has a small amplitude, we can use a first order Taylor series approximation of the hyperbolic tangent ($\tanh\frac{z}{2} \approx \frac{z}{2}$) as follows:

$$i_1 \approx \frac{I_k}{2}\left[1+\frac{z}{2}\right]=\frac{I_k}{2}+\frac{g_{in}}{2}(v_1-v_2) \quad \text{where} \quad g_{in}=\frac{q\left(\frac{I_k}{2}\right)}{kT}$$ is the input conductance of a transistor biased by an emitter current equal to $\frac{I_k}{2}$ (seen from the emitter). The other current is $i_2 \approx \frac{I_k}{2}\left[1-\frac{z}{2}\right]=\frac{I_k}{2}-\frac{g_{in}}{2}(v_1-v_2)$.

Since the output current is $i_{Ck} = \alpha i_k$, we can define the small signal transconductance as:

$$g_m=\frac{\alpha g_{in}}{2}$$

So, we can remark that the gain of the differential pair is half of the gain of a single ended transistor biased by an emitter current equal to $\frac{I_k}{2}$.

If $(v_1-v_2)=V_1\cos\omega_0 t$, we can develop the current i in Fourier series.

$z=\frac{qV_1}{kT}\cos\omega_0 t = x\cos\omega_0 t$ giving:

$$i=\frac{I_k}{2}\tanh\left[\frac{x}{2}\cos\omega_0 t\right] \qquad (15)$$

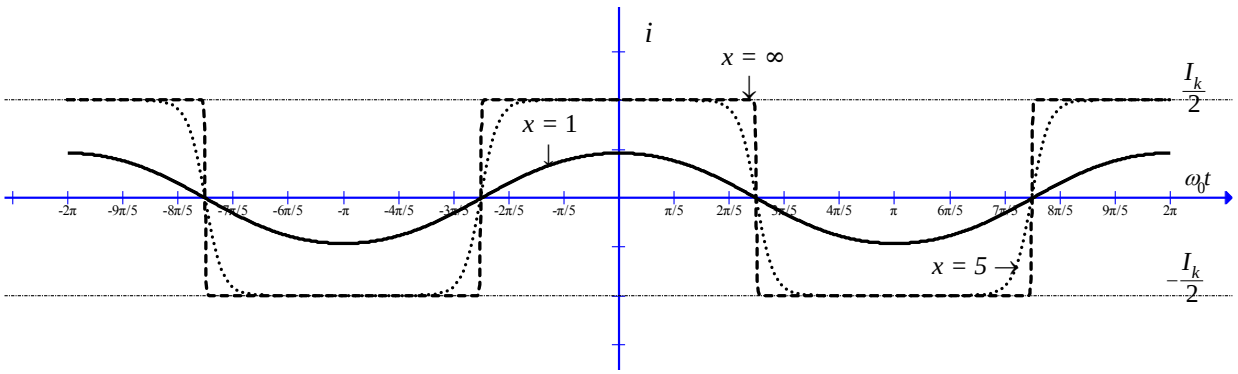


Fig.3- 17 Sketch of *i* for several values of *x*

The above sketch shows the shape of the current *i* for several values of *x*. It goes from a sinusoidal shape for small input to a square wave when the input becomes large. Equation (15) represents a periodic waveform. Its Fourier series is given by:

$$i=\sum_{n=1}^{\infty} I_{2n-1}\cos(2n-1)\omega_0 t$$

$$=I_k\sum_{n=1}^{\infty} a_{2n-1}(x)\cos(2n-1)\omega_0 t$$

The coefficients are tabulated in p.117 of the textbook. This table is reproduced below.

x	$a_1(x) = I_1/I_k$	$a_3(x) = I_3/I_k$	$a_5(x) = I_5/I_k$
0.0	0.0000	0.0000	0.0000
0.5	0.1231	—	—
1.0	0.2356	−0.0046	—
1.5	0.3305	−0.0136	—
2.0	0.4058	−0.0271	—
2.5	0.4631	−0.0435	0.00226
3.0	0.5054	−0.0611	0.0097
4.0	0.5586	—	—
5.0	0.5877	−0.1214	0.0355
7.0	0.6112	−0.1571	0.0575
10.0	0.6257	−0.1827	0.0831
∞	0.6366	−0.2122	+0.1273

Fig.3- 18 Normalized harmonics

The last row of the above table represents in fact the Fourier series development of a square wave having zero dc and peak amplitude of ½.

If we use a tank circuit as a load for one of the transistors, we can use the large signal transconductance. This transconductance is defined as:

$$G_m(x) = \frac{\alpha I_1}{V_1} = \frac{\alpha\left(I_k a_1(x)\right)}{\left(x\frac{kT}{q}\right)} = 2\alpha g_{in}\frac{a_1(x)}{x} = g_m\frac{4a_1(x)}{x}$$

It is represented in the figure below.

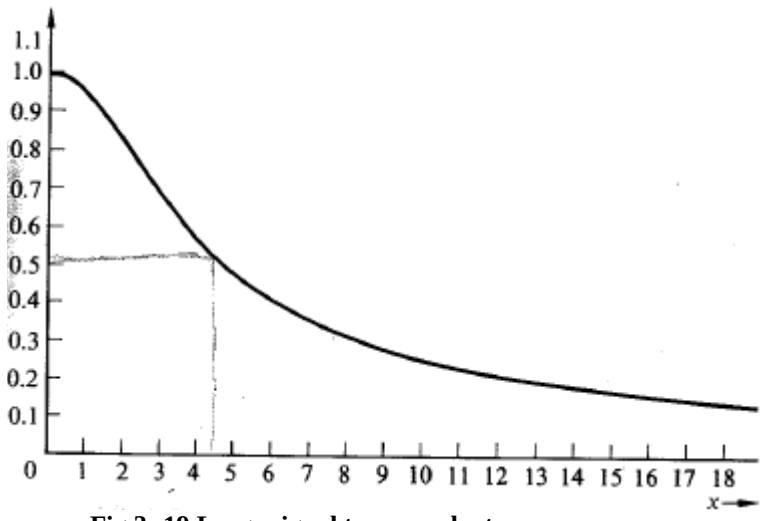


Fig.3- 19 Large signal transconductance vs *x*

Here again, we see the decrease of the gain as the input amplitude increases.

3.6 Effect of series resistance

When a resistance *R* is connected in series with a nonlinear element, it has the net effect of making the characteristics practically (piecewise) linear. In this section, we are going to study the effect of the resistance on the exponential characteristics. The same analysis can be repeated on other nonlinearities such as the square law.

Consider the following circuit:

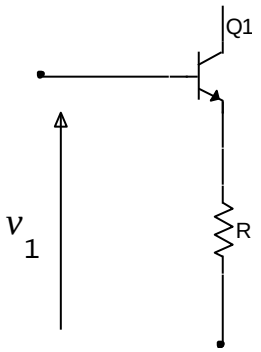


Fig.3- 20 NPN transistor with series resistance in the emitter

From Fig.3- 20, we can write:

$$v_1 = v_{BE} + Ri_E$$

and the transistor is described by the exponential characteristic: $i_E = I_{ES}\exp\left(\frac{qv_{BE}}{kT}\right)$ or $v_{BE} = \frac{kT}{q}\ln\left(\frac{i_E}{I_{ES}}\right)$. This gives:

$$v_1 = \frac{kT}{q}\ln\left(\frac{i_E}{I_{ES}}\right) + Ri_E$$

We can define a small signal dynamic resistance as:

$$r_{in}' = \left.\frac{dv_1}{di_E}\right|_{i_E = I_{dc}} = \frac{kT}{qI_{dc}} + R = r_{in} + R$$

The output current being the collector current, the small signal transconductance of the compound device is:

$$g_m' = \frac{\alpha}{r_{in}'} = \frac{\alpha}{r_{in} + R} = \frac{\alpha g_{in}}{1 + g_{in}R}$$

$g_{in} = 1/r_{in}$ is the small signal dynamic conductance (seen from the emitter).

We can remark that the small signal gain decreases with increasing *R*. To show the effect of piecewise linearization, let us introduce the dc current flowing in the emitter circuit.

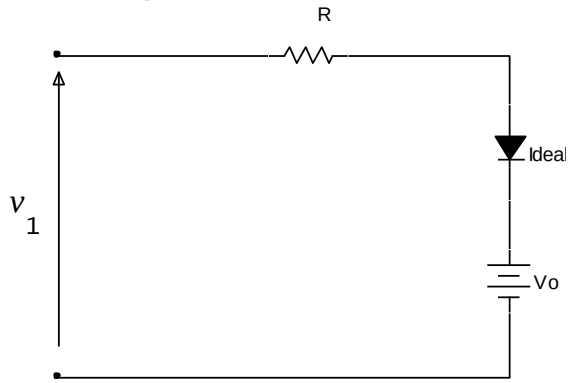
$$v_1 = \frac{kT}{q}\ln\left(\frac{i_E}{I_{ES}}\frac{I_{dc}}{I_{dc}}\right) + Ri_E = \frac{kT}{q}\ln\left(\frac{I_{dc}}{I_{ES}}\right) + \frac{kT}{q}\ln\left(\frac{i}{I_{dc}}\right) + Ri_E$$

Let $V_0 = \frac{kT}{q}\ln\left(\frac{i_E}{I_{ES}}\right)$ and $V_{co} = I_{dc}(r_{in} + R) = \frac{kT}{q}(1 + g_{in}R)$, the above expression can be evaluated as:

$$\frac{v_1 - V_0}{V_{co}} = \left[\frac{g_{in}R}{1 + g_{in}R}\right]\left(\frac{i_E}{I_{dc}}\right) + \frac{\ln\left(i_E / I_{dc}\right)}{1 + g_{in}R} \qquad (16)$$

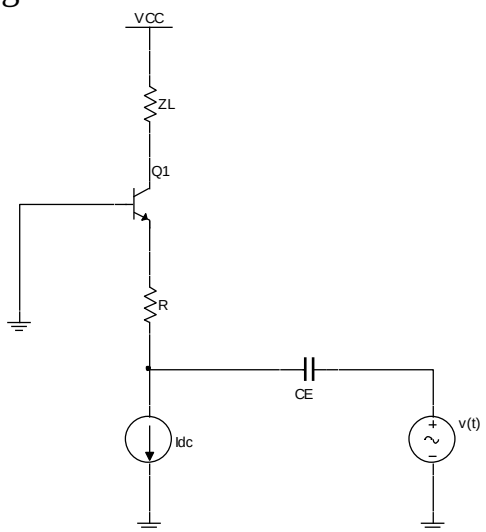
Two extreme cases for equation (16) are of interest. The first one corresponds to $g_{in}R = 0$. This is the case of the exponential characteristics seen in section 3.3. The other extreme case corresponds to $g_{in}R = \infty$. In this case, the second term in the above expression will be zero and we obtain:

$\frac{v_1 - V_0}{V_{co}} = \frac{i_E}{I_{dc}}$ for $v_1 > V_0$ and of course, no current can flow if $v_1 < V_0$. In this case, $R >> r_{in}$ and $V_{co} = RI_{dc}$. Finally, the piecewise linear characteristic is the one of an ideal diode in series with a battery of value V_0 and a resistance R. The base emitter is replaced by the following circuit:

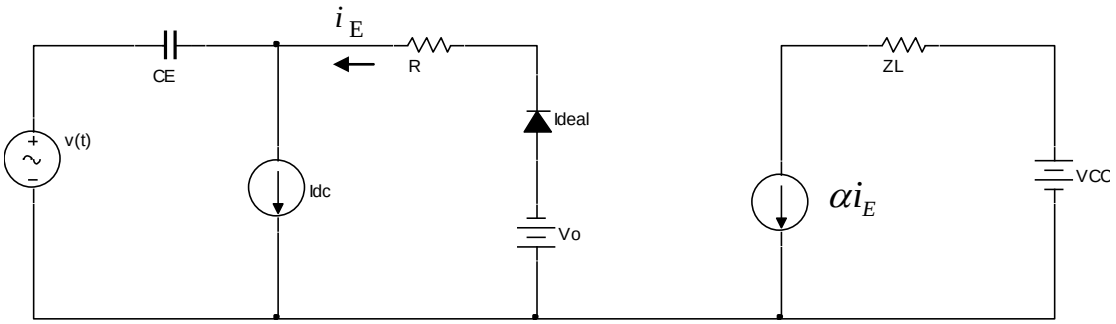


The current flowing in the above circuit is of course the emitter current.

Consider the following circuit:



It can be analyzed using the following equivalent circuit:



The capacitor is going to develop a biasing voltage V_b that will be added to the input ac voltage $v(t) = V_1 \cos \omega_0 t$. The average value of the emitter current is fixed by the dc current source. So, we will have the following situation:

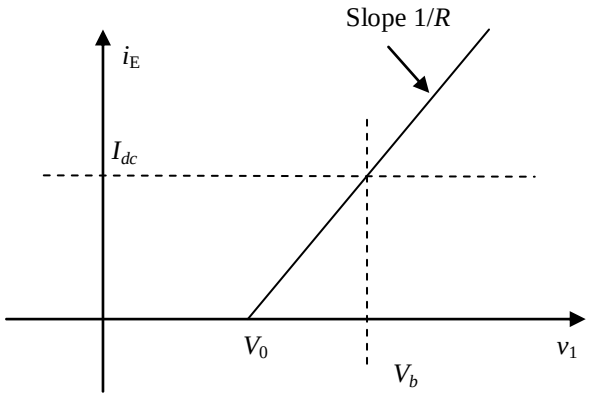


Fig.3- 21 Input transfer

The voltage applied to the resistance in series with the base emitter junction is: $v_1 = V_b + V_1 \cos \omega_0 t$. From the above figure, it is clear that if the amplitude of the ac input voltage satisfies: $V_1 \le RI_{dc} = V_{co}$, we are in the class A and the emitter current satisfies:

$$i_E = I_{dc} + \frac{V_1}{R} \cos \omega_0 t = I_0 + I_1 \cos \omega_0 t = I_{dc} \left[1 + \frac{V_1}{V_{co}} \cos \omega_0 t \right]$$

When $V_1 > V_{co}$, we leave the class A and the current becomes a periodic train of sinewave tips as seen in section 3.1. The dc value of the current is fixed by the biasing network. However, since the current is now asymmetrical, the voltage across the capacitor is going to move in order to maintain the current at its biasing value I_{dc}.

$$i_E = I_0 + I_1 \cos \omega_0 t + I_2 \cos 2\omega_0 t + \cdots$$

From the equations developed in section 3.1, we have:

$$I_0 = I_{dc} = \frac{V_1 - V_x}{\pi R}\frac{\sin\phi - \phi\cos\phi}{1-\cos\phi}$$

$$I_1 = \frac{V_1 - V_x}{\pi R}\frac{\phi - \cos\phi\sin\phi}{1-\cos\phi}$$

while $\phi = \cos^{-1}\frac{V_x}{V_1}$ and $V_x = V_b - V_0$.

Using the fact that $V_1 - V_x = V_1(1-\cos\phi)$, we can relate V_1/V_{co} to ϕ by:

$$\frac{V_1}{V_{co}} = \frac{\pi}{\sin\phi - \phi\cos\phi} \tag{17}$$

and

$$\frac{I_1}{I_0} = \frac{\phi - \sin\phi\cos\phi}{\sin\phi - \phi\cos\phi} \tag{18}$$

The above two equations form a parametric evaluation of the relation between I_1/I_{dc} and V_1/V_{co} for $V_1 > V_{co}$ and using the result of class A also ($I_1/I_{dc} = V_1/V_{co}$), we can plot the following curve:

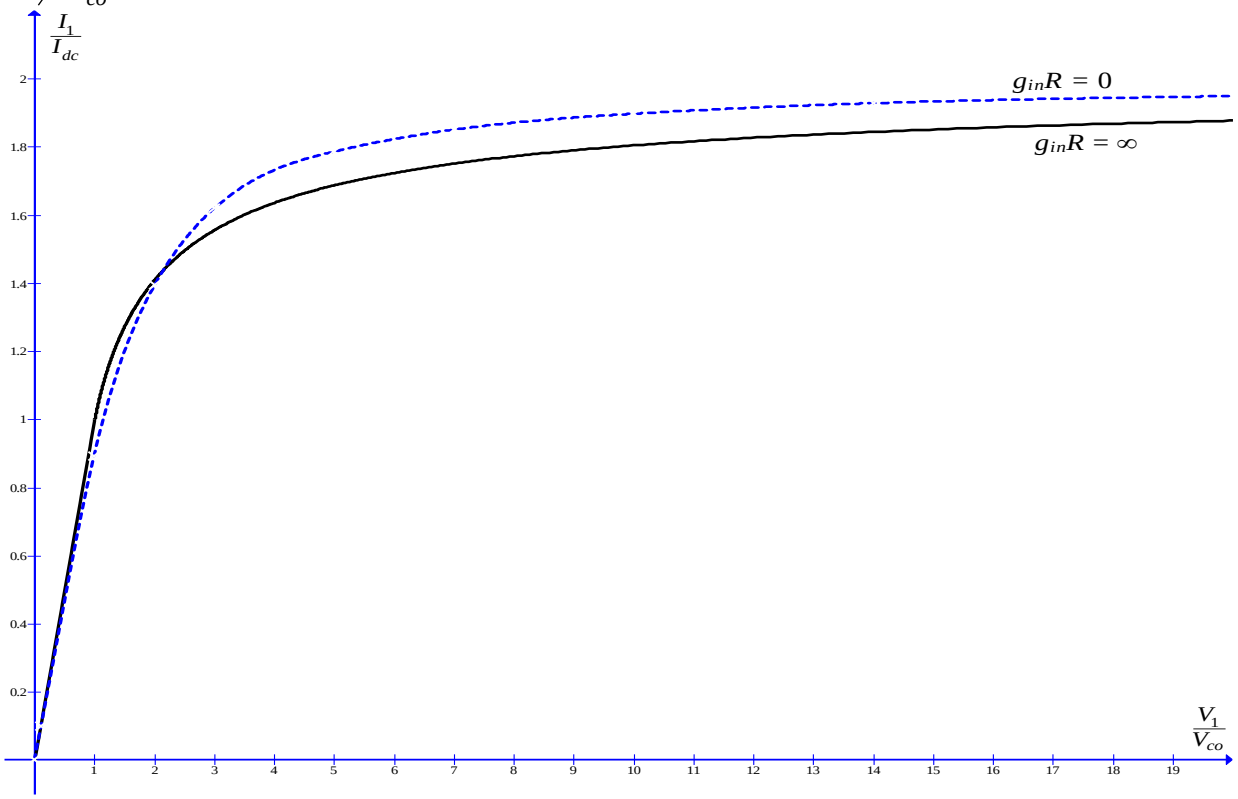


Fig.3- 22 Normalized fundamental vs. normalized input voltage

In the above graph, two curves are drawn: the one corresponding to $g_{in}R = \infty$ and the one corresponding to $g_{in}R = 0$. The second one is just the curve

expressing $2I_1(x)/I_0(x)$ vs. *x*. This is due to the fact that $V_{co} = r_{in} I_{dc} = \frac{kT}{q}$ in this case, so $\frac{V_1}{V_{co}} = \frac{qV_1}{kT} = x$. We can use the above set for any value of *R* by interpolating between the two curves.

If the load of the transistor is a high Q tank circuit, here again, we can use the concept of large signal transconductance.

$$G_m = \frac{\alpha I_1}{V_1} = \frac{I_1}{I_{dc}} \frac{V_{co}}{V_1} \frac{\alpha I_{dc}}{V_{co}} = \frac{\left(I_1/I_{dc}\right)}{\left(V_1/V_{co}\right)} g_m'$$

$g_m' = \frac{\alpha I_{dc}}{V_{co}} = \frac{\alpha I_{dc}}{(r_{in} + R) I_{dc}}$ is the small signal transconductance evaluated at the Q point. We can use the previous set of curves (Fig.3- 22) to draw the curve giving G_m/g_m', for different values of V_1/V_{co}. This can be done for the two cases: $g_{in}R = \infty$ and $g_{in}R = 0$.

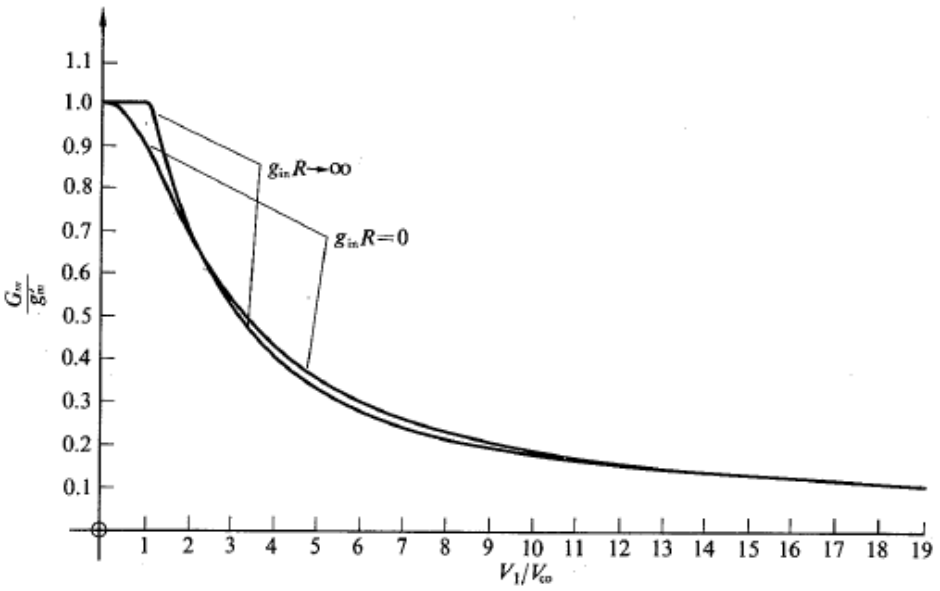
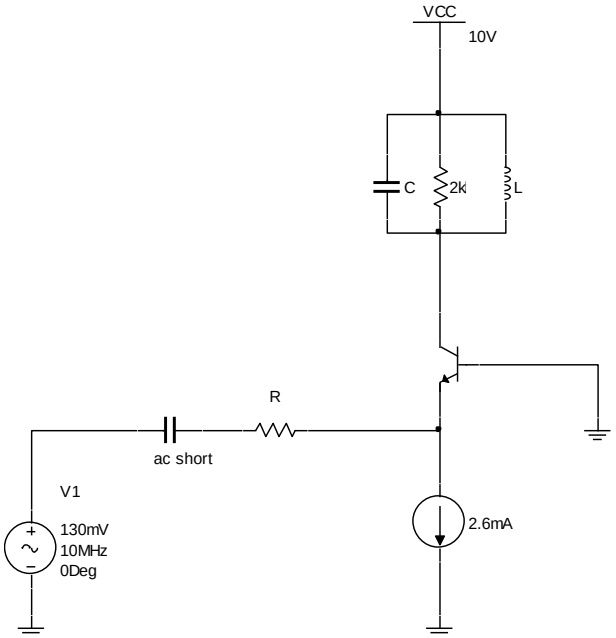


Fig.3- 23 Normalized large signal transconductance vs. normalized input voltage

We see here again the decrease of the gain as the distortion of the output current increases. Consider the following circuit:



The tank circuit composed of L and C is tuned a 10 MHz. We assume that $\alpha \approx 1$. We will compute the output voltage for the three cases: R = 10 Ω, R = 0 and R = 100 Ω.

First, we compute g_{in} and r_{in}.

I_{dc} = 2.6 mA gives $g_{in} = \dfrac{qI_{dc}}{kT} = \dfrac{2.6mA}{26mV} = 0.1\Omega^{-1}$, so $r_{in} = 10\Omega$.

Case R = 10 Ω: $g_{in}R = 1$. We must compute V_{co}.

$V_{co} = I_{dc}\left(r_{in} + R\right) = \left(2.6mA\right) \times \left(20\Omega\right) = 52mV$.

$\dfrac{V_1}{V_{co}} = \dfrac{130}{52} = 2.5$. From the curves in Fig.3- 22, we read $\dfrac{I_1}{I_{dc}} = 1.5$. The fundamental of the output current is then: $I_1 = 1.5 \times \left(2.6mA\right) = 3.9mA$. So, the voltage at the collector of the transistor is:

$$v_o(t) = 10V + \left(2k\Omega\right) \times \left(3.9mA\right)\cos\left(2\pi 10^7 t\right) = 10V + \left(7.8V\right)\cos\left(2\pi 10^7 t\right)$$

Case R = 0: $g_{in}R = 0$. We have $V_{co} = 26mV$. We obtain: $\dfrac{V_1}{V_{co}} = \dfrac{130}{26} = 5$ giving $\dfrac{I_1}{I_{dc}} = 1.8$ from the curve $g_{in}R = 0$. In this case, the output voltage is:

$$v_o(t) = 10V + \left(9.36V\right)\cos\left(2\pi 10^7 t\right)$$

Case R = 100 Ω. $g_{in}R = 10$. This value is quite large.

$V_{co} = (2.6mA) \times (10\Omega + 100\Omega) = 286mV$. In this case, we have $V_1 < V_{co}$. So, $I_1 = g_m' V_1 = \frac{130mV}{110\Omega} = 1.18mA$. The output voltage is:

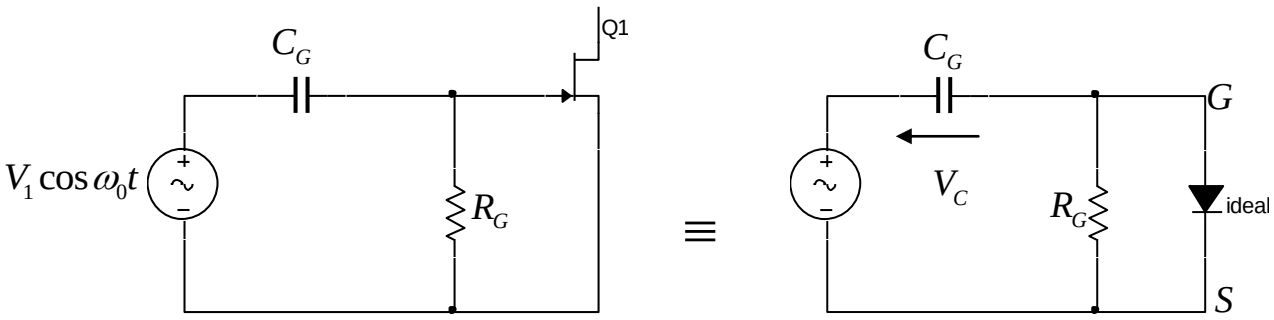
$$v_o(t) = 10 + (2.36V)\cos(2\pi 10^7 t)$$

If we double the input voltage (V_1 = 260 mV), we will still have $V_1 < V_{co}$. The amplification will still be linear.

3.7 Clamp biased FET

We have seen that N channel junction FET must be biased with a negative V_{GSQ} to keep the gate to channel diode reverse biased. One technique for automatically achieving this is to use clamp biasing.

Consider the following circuit:



The circuit is equivalent to the one on the right. We assume that the time constant of the RC network satisfies $R_G C_G >> \frac{2\pi}{\omega_0}$. In this case, the capacitor will charge to the peak value of the input sinewave ($V_C = V_1$) and it will not discharge. So, the voltage v_{GS} will satisfy:

$$v_{GS} = V_1 \cos \omega_0 t - V_C = V_1 (\cos \omega_0 t - 1)$$

The above equation show clearly that the voltage v_{GS} is going to be clamped to zero and it will remain negative. If $V_1 \le \frac{|V_p|}{2}$, the FET will be operated completely in the square region. If $V_1 > \frac{|V_p|}{2}$, the drain current will consist of squared sine tips of peak value $I_p = I_{DSS}$ and it will contain more harmonics.

$$i_D = I_0 + I_1 \cos \omega_0 t + I_2 \cos 2\omega_0 t + I_3 \cos 3\omega_0 t + \cdots$$

The following two curves provide the values of the first components of the current along with the normalized transconductance.

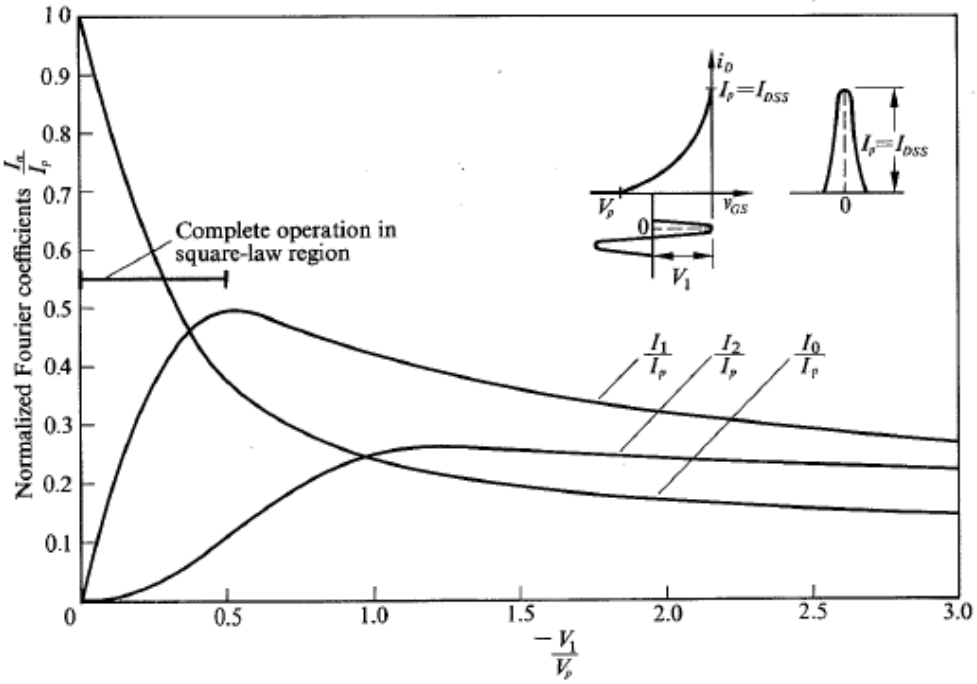


Fig.3- 24 Normalized Fourier Coefficients

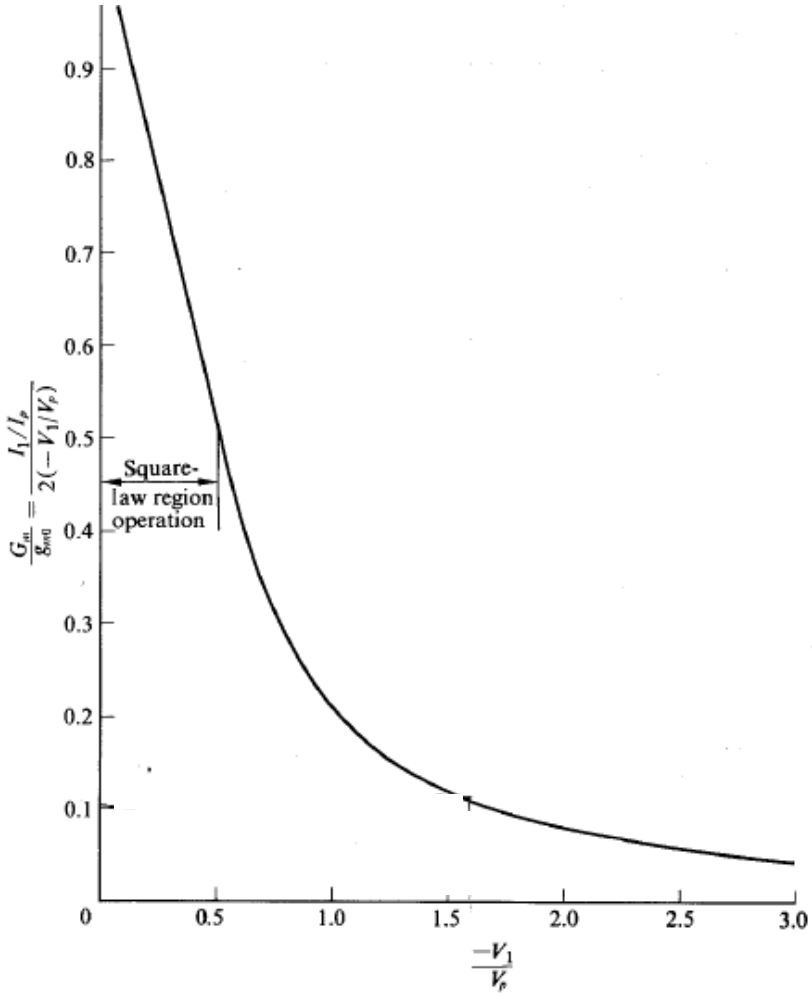


Fig.3- 25 Large signal transconductance

The large signal transconductance is normalized to $g_{m0} = \frac{-2I_{DSS}}{V_p}$.

For example, consider an FET with I_{DSS} = 6 mA and V_p = –4 V. If we apply an input voltage $v(t) = (2\,V)\cos\omega_0 t$, we have $-V_1/V_p = 0.5$. From the curve in Fig.3- 24, the normalized fundamental current is $I_1/I_{DSS} = 0.5$, giving a fundamental current $(3mA)\cos\omega_0 t$.

3.8 Non linear loading of tank circuits

It is quite common that the input of the different nonlinear controlled sources is tuned using a parallel tank circuit. If the Q of the tank circuit is high enough, the voltage across the circuit will be sinusoidal, even if the current absorbed by the nonlinear load is not. Since all the harmonics produced by the load will be absorbed (shorted to ground) by the tank circuit, the nonlinear load will behave like an equivalent conductance G_{NL} given by:

$G_{NL} = \frac{I_1}{V_1}$ where I_1 is the amplitude of the fundamental current absorbed by the load and V_1 is the amplitude of the sinusoidal voltage across the load.

<u>Common base equivalent input:</u>

Let us consider the following circuit:

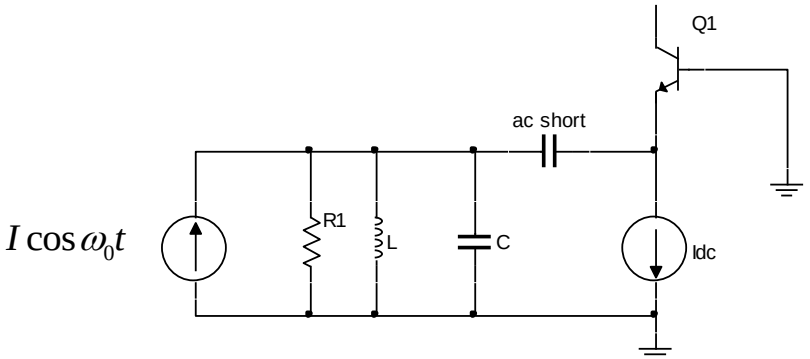


Fig.3- 26 Tank circuit at emitter

We assume that $\omega_0^2 = 1/LC$ and that the Q of the tank circuit is high enough in order to keep the voltage across it sinusoidal. We have seen that the emitter current of the transistor is given by:

$$i_E(t) = I_{dc}\left[1 + \sum_{n=1}^{\infty} \frac{2I_n(x)}{I_0(x)}\cos n\omega_0 t\right]$$

where $x = \frac{qV_1}{kT}$ and $V_1\cos\omega_0 t$ is the sinusoidal voltage appearing across the tank circuit.

The fundamental current has an amplitude: $I_1 = I_{dc}\dfrac{2I_1(x)}{I_0(x)}$ and the base emitter junction will behave like a conductance:

$$G_{NL} = \frac{I_1}{V_1} = \frac{2I_{dc}I_1(x)}{V_1 I_0(x)} = \frac{qI_{dc}}{kT}\frac{2I_1(x)}{xI_0(x)} = \frac{G_m(x)}{\alpha}$$

We must verify that the Q is high enough:

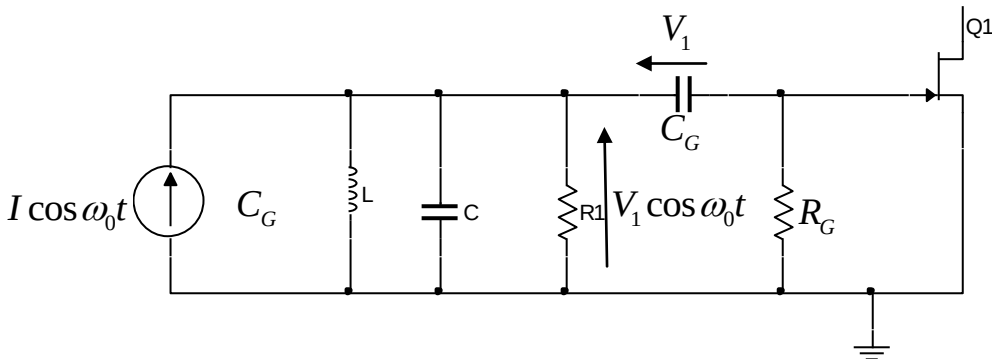
$$Q = \frac{C\omega_0}{G_1 + G_{NL}} \geq 10 \text{ where } G_1 = \frac{1}{R_1}$$

Common emitter equivalent input:

If we consider now the base emitter junction, but seen from the base, the current is smaller $i_B = (1-\alpha)i_E$. So, the conductance is:

$$G_{NL} = (1-\alpha)\frac{G_m(x)}{\alpha} = \frac{G_m(x)}{\beta}$$

Clamp biased FET equivalent input:



The current flowing in the gate channel diode consists of very short impulses occurring at each peak of the sinewave $V_1\cos\omega_0 t$. This means that we can develop this gate current in the following Fourier series:

$$i_G = I_{dc}\left[1 + 2\sum_{n=1}^{\infty}\cos n\omega_0 t\right]$$

Since no dc current can flow through the capacitor, this dc current is going to flow through the resistor R_G. The dc voltage across R_G is the peak value V_1 of the ac voltage stored in the capacitor C_G. So:

$I_{dc} = \dfrac{V_1}{R_G}$ and the amplitude of the fundamental current in this diode is then: $2\dfrac{V_1}{R_G}$. There is also an ac current of amplitude $\dfrac{V_1}{R_G}$ at ω_0 flowing in this resistance since there is an ac voltage $V_1\cos\omega_0 t$ across it. The total ac current at

ω_0 flowing inside the circuit is then the sum of the two currents. Finally, the equivalent conductance across the tank circuit is:

$$G_{NL} = \frac{\frac{3V_1}{R_G}}{V_1} = \frac{3}{R_G}$$